

High speed serial link design (SERDES)

Introduction, Architectures and applications

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Abstract This paper describes basic methods of transferring data through serial data buses, using serializer-deserializer (SerDes) as main device in this operation. It explains function of SerDes and different techniques for implementing it.

Keywords: SERDES, Clock and data recovery, High speed SerDes, Parallel clock SERDES, Embedded clock SERDES, Shared SERDES, Bit interleaving SERDES

I. INTRODUCTION

The simplest method of transferring data through the inputs or outputs of a silicon chip is to directly connect the datapath from one chip to the next chip. Since data often consist of more than one bit of information, the datapath is more than one-bit wide.

There are two inherent problems of the parallel data bus. The first problem is that n input/output (I/O) pins are required on each chip to transfer the data. The second problem involves meeting timing requirements. Due to these two problems we thought about transforming parallel data to serial streams of data to be able to use serial communications off-chips and on-chips.

Serializers/Deserializers (SerDes) are the main devices which convert parallel data into stream of serial data and send it through a channel.

Serial interconnects form the critical backbone of modern communication systems, so the choice of SerDes can have a big impact on system cost and performance. While the range of choices may seem confusing at first, SerDes devices fall into a few basic architectures, each tailored to specific application requirements. A basic understanding of these architectural differences enables the designer to quickly find the right SerDes for the application. In this paper we examine four distinct SerDes architectures and show how each plays a vital role in today's systems.

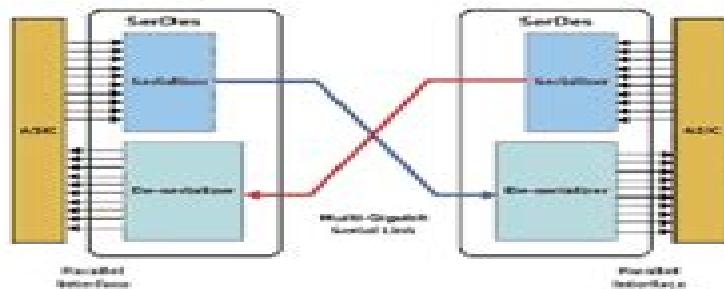


Fig. 1 serial-to-parallel device

II. ARCHITECTURE OF HIGH-SPEED SERDES

High-speed Serializer/Deserializer (HSS) devices are the dominant implementation of I/O interfaces at speed of 2.5 Gbps and higher. Such devices are differentiated from source-synchronous interface in that the receiver device contains a clock data recovery (CDR) circuit dynamically determines the optimal sampling point of the data signal based upon the transition edges of the signal. In other words clock information is extracted directly from the data rather than relying on a separate clock.



Fig. 2 HSS basic block diagram

Fig. 2 illustrate the basic block diagram of the transmit and receive channels of an HSS device. The transmitter serializes parallel data, equalizes it and then drives the serial data onto a differential signal pair of interconnect wires. The receiver consists of a differential receiver, a CDR circuit which may also integrate an equalizer and deserializes the data upon the sample point established by the CDR.

SerDes cores which contain only transmit or only receive channels are called **simplex cores**; SerDes cores which contain both transmit and receive channels are called **full duplex cores**. Note that the terminology "full duplex" does not imply that the electrical interface is bidirectional. Any given electrical interconnect channel has a fixed direction of data transmission. If a protocol application requires "full duplex" communication, then independent transmit and receive channels with independent interconnections are used to implement the interface.



Simplex core, no Rx block



Full Duplex Core, Rx and Tx over Channel A



Full Duplex Core, Rx and Tx over Channel A and B

Fig. 3 different types of serdes cores

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Efficient Test Methodologies for High-Speed Serial Links Dongwoo Hong,Kwang-Ting Cheng,2009-12-24 Efficient Test Methodologies for High Speed Serial Links describes in detail several new and promising techniques for cost effectively testing high speed interfaces with a high test coverage One primary focus of Efficient Test Methodologies for High Speed Serial Links is on efficient testing methods for jitter and bit error rate BER which are widely used for quantifying the quality of a communication system Various analysis as well as experimental results are presented to demonstrate the validity of the presented techniques

High Speed Serdes Devices and Applications David Robert Stauffer,Jeanne Trinko Mechler,Michael A. Sorna,Kent Dramstad,Clarence Rosser Ogilvie,Amanullah Mohammad,James Donald Rockrohr,2008-12-19 The simplest method of transferring data through the inputs or outputs of a silicon chip is to directly connect each bit of the datapath from one chip to the next chip Once upon a time this was an acceptable approach However one aspect and perhaps the only aspect of chip design which has not changed during the career of the authors is Moore's Law which has dictated substantial increases in the number of circuits that can be manufactured on a chip The pin densities of chip packaging technologies have not increased at the same pace as has silicon density and this has led to a prevalence of High Speed Serdes HSS devices as an inherent part of almost any chip design HSS devices are the dominant form of input output for many if not most high integration chips moving serial data between chips at speeds up to 10 Gbps and beyond Chip designers with a background in digital logic design tend to view HSS devices as simply complex digital input output cells This view ignores the complexity associated with serially moving billions of bits of data per second At these data rates the assumptions associated with digital signals break down and analog factors demand consideration The chip designer who oversimplifies the problem does so at his or her own peril

High Speed VCSELs for Optical Interconnects Alex Mutig,2011-01-12 The transmission speed of data communication systems is forecast to increase exponentially over the next decade Development of both Si based high speed drivers as well as III V semiconductor based high speed vertical cavity surface emitting lasers VCSELs are prerequisites for future ultrahigh data rate systems This thesis presents a survey of the present state of the art of VCSELs a systematic investigation of the various effects limiting present VCSELs a catalogue of solutions to overcome present limits detailed progress in modelling fabricating and testing the currently most advanced VCSELs at the two commercially most important wavelengths

Machine Learning-based Design and Optimization of High-Speed Circuits Vazgen Melikyan,2023-12-30 This book describes machine learning based new principles methods of design and optimization of high speed integrated circuits included in one electronic system which can exchange information between each other up to 128 256 512 Gbps speed The efficiency of methods has been proven and is described on the examples of practical designs This will enable readers to use them in similar electronic system designs The author demonstrates newly developed principles and methods to accelerate communication between ICs working in non standard operating conditions considering signal

deviation compensation with linearity self calibration The observed circuit types also include but are not limited to mixed signal high performance heterogeneous integrated circuits as well as digital cores **DFCCIL Executive Exam**

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Robertazzi,1993-05-05 A handy source for practicing engineers and researchers this book offers collected examples of successful performance evaluation of high speed telecommunications switching fabrics such as ATM networks and high speed interconnection technology for computers It emphasizes the performance evaluation of such switches as they apply to predicting a proposed system s performance through the use of statistical models a cost saving way for communications engineers to test the design of a system without having to construct it

Conference Record ,2003 High-Speed

Signaling Kyung Suk (Dan) Oh,Xing Chao (Chuck) Yuan,2011-10-07 New System Level Techniques for Optimizing Signal Power Integrity in High Speed Interfaces from Pioneering Innovators at Rambus Stanford Berkeley and MIT As data communication rates accelerate well into the multi gigahertz range ensuring signal integrity both on and off chip has become crucial Signal integrity can no longer be addressed solely through improvements in package or board level design Diverse engineering teams must work together closely from the earliest design stages to identify the best system level solutions In High Speed Signaling several of the field s most respected practitioners and researchers introduce cutting edge modeling simulation and optimization techniques for meeting this challenge Edited by pioneering experts Drs Dan Oh and Chuck Yuan these contributors explain why noise and jitter are no longer separable demonstrate how to model their increasingly complex interactions and thoroughly introduce a new simulation methodology for predicting link level performance with unprecedented accuracy The authors address signal integrity from architecture through high volume production thoroughly discussing design implementation and verification Coverage includes New advances in passive channel modeling power supply noise and jitter modeling and system margin prediction Methodologies for balancing system voltage and timing budgets to improve system robustness in high volume manufacturing Practical stable formulae for converting key network parameters Improved solutions for difficult problems in the broadband modeling of interconnects Equalization techniques for optimizing channel performance Important new insights into the relationships between jitter and clocking topologies New on chip measurement techniques for in situ link performance testing Trends and future directions in signal integrity engineering High Speed Signaling thoroughly introduces new techniques pioneered at Rambus and other leading high tech companies and universities approaches that have never before been presented with this much practical detail It will be invaluable to everyone concerned with signal integrity including signal and power integrity engineers high speed I O circuit designers and system level board design engineers

IEEE VLSI Test Symposium ,2004 2004 IEEE Nuclear Science Symposium

Conference Record ,2004 Life-Cycle of Engineering Systems: Emphasis on Sustainable Civil Infrastructure Jaap Bakker,Dan M. Frangopol,Klaas Breugel,2016-11-18 This volume contains the papers presented at IALCCE2016 the fifth International Symposium on Life Cycle Civil Engineering IALCCE2016 to be held in Delft The Netherlands October 16 19 2016 It consists of a book of extended abstracts and a DVD with full papers including the Fazlur R Khan lecture keynote lectures and technical papers from all over the world All major aspects of life cycle engineering are addressed with special

focus on structural damage processes life cycle design inspection monitoring assessment maintenance and rehabilitation life cycle cost of structures and infrastructures life cycle performance of special structures and life cycle oriented computational tools The aim of the editors is to provide a valuable source for anyone interested in life cycle of civil infrastructure systems including students researchers and practitioners from all areas of engineering and industry Journal of Southeast University ,2004 Electronic Design ,2001 Network Congestion Control Michael Welzl,2005-09-02 As the Internet becomes increasingly heterogeneous the issue of congestion control becomes ever more important In order to maintain good network performance mechanisms must be provided to prevent the network from being congested for any significant period of time Michael Welzl describes the background and concepts of Internet congestion control in an accessible and easily comprehensible format Throughout the book not just the how but the why of complex technologies including the Transmission Control Protocol TCP and Active Queue Management are explained The text also gives an overview of the state of the art in congestion control research and an insight into the future Network Congestion Control Presents comprehensive easy to read documentation on the advanced topic of congestion control without heavy maths Aims to give a thorough understanding of the evolution of Internet congestion control how TCP works why it works the way it does and why some congestion control concepts failed for the Internet Explains the Chiu Jain vector diagrams and introduces a new method of using these diagrams for analysis teaching design Elaborates on how the theory of congestion control impacts on the practicalities of service delivery Includes an appendix with examples problems to assist learning Provides an accompanying website with Java tools for teaching congestion control as well as examples links to code and projects bibliography This invaluable text will provide academics and researchers in computer science electrical engineering and communications networking as well as students on advanced networking and Internet courses with a thorough understanding of the current state and future evolution of Internet congestion control Network administrators and Internet service and applications providers will also find Network Congestion Control a comprehensive accessible self teach tool

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Table of Contents Pdf High Speed Serial Link Measurement

1. Understanding the eBook Pdf High Speed Serial Link Measurement
 - The Rise of Digital Reading Pdf High Speed Serial Link Measurement
 - Advantages of eBooks Over Traditional Books
2. Identifying Pdf High Speed Serial Link Measurement
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in an Pdf High Speed Serial Link Measurement
 - User-Friendly Interface
4. Exploring eBook Recommendations from Pdf High Speed Serial Link Measurement
 - Personalized Recommendations
 - Pdf High Speed Serial Link Measurement User Reviews and Ratings
 - Pdf High Speed Serial Link Measurement and Bestseller Lists
5. Accessing Pdf High Speed Serial Link Measurement Free and Paid eBooks
 - Pdf High Speed Serial Link Measurement Public Domain eBooks
 - Pdf High Speed Serial Link Measurement eBook Subscription Services
 - Pdf High Speed Serial Link Measurement Budget-Friendly Options
6. Navigating Pdf High Speed Serial Link Measurement eBook Formats
 - ePUB, PDF, MOBI, and More
 - Pdf High Speed Serial Link Measurement Compatibility with Devices
 - Pdf High Speed Serial Link Measurement Enhanced eBook Features
7. Enhancing Your Reading Experience
 - Adjustable Fonts and Text Sizes of Pdf High Speed Serial Link Measurement
 - Highlighting and Note-Taking Pdf High Speed Serial Link Measurement
 - Interactive Elements Pdf High Speed Serial Link Measurement
8. Staying Engaged with Pdf High Speed Serial Link Measurement

- Joining Online Reading Communities
- Participating in Virtual Book Clubs
- Following Authors and Publishers Pdf High Speed Serial Link Measurement

9. Balancing eBooks and Physical Books Pdf High Speed Serial Link Measurement

- Benefits of a Digital Library
- Creating a Diverse Reading Collection Pdf High Speed Serial Link Measurement

10. Overcoming Reading Challenges

- Dealing with Digital Eye Strain
- Minimizing Distractions
- Managing Screen Time

11. Cultivating a Reading Routine Pdf High Speed Serial Link Measurement

- Setting Reading Goals Pdf High Speed Serial Link Measurement
- Carving Out Dedicated Reading Time

12. Sourcing Reliable Information of Pdf High Speed Serial Link Measurement

- Fact-Checking eBook Content of Pdf High Speed Serial Link Measurement
- Distinguishing Credible Sources

13. Promoting Lifelong Learning

- Utilizing eBooks for Skill Development
- Exploring Educational eBooks

14. Embracing eBook Trends

- Integration of Multimedia Elements
- Interactive and Gamified eBooks

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