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Microarchitecture of Network-on- Chip Routers

A Designer's Perspective

 Springer

Microarchitecture Of Network On Chip Routers A Designers Perspective

**Lennart Bamberg, Jan Moritz
Joseph, Alberto García-Ortiz, Thilo
Pionteck**



Microarchitecture Of Network On Chip Routers A Designers Perspective:

Microarchitecture of Network-on-Chip Routers Giorgos Dimitrakopoulos, Anastasios Psarras, Ioannis Seitanidis, 2014-08-27 This book provides a unified overview of network on chip router micro architecture the corresponding design opportunities and challenges and existing solutions to overcome these challenges The discussion focuses on the heart of a NoC the NoC router and how it interacts with the rest of the system Coverage includes both basic and advanced design techniques that cover the entire router design space including router organization flow control pipelined operation buffering architectures as well as allocators structure and algorithms Router micro architectural options are presented in a step by step manner beginning from the basic design principles Even highly sophisticated design alternatives are categorized and broken down to simpler pieces that can be understood easily and analyzed This book is an invaluable reference for system architecture circuit and EDA researchers and developers who are interested in understanding the overall picture of NoC routers architecture the associated design challenges and the available solutions

3D Interconnect Architectures for Heterogeneous Technologies Lennart Bamberg, Jan Moritz Joseph, Alberto García-Ortiz, Thilo Pionteck, 2022-06-27 This book describes the first comprehensive approach to the optimization of interconnect architectures in 3D systems on chips SoCs specially addressing the challenges and opportunities arising from heterogeneous integration Readers learn about the physical implications of using heterogeneous 3D technologies for SoC integration while also learning to maximize the 3D technology gains through a physical effect aware architecture design The book provides a deep theoretical background covering all abstraction levels needed to research and architect tomorrow s 3D integrated circuits an extensive set of optimization methods for power performance area and yield as well as an open source optimization and simulation framework for fast exploration of novel designs

Designing Network On-Chip Architectures in the Nanoscale Era Jose Flich, Davide Bertozzi, 2010-12-18 Going beyond isolated research ideas and design experiences Designing Network On Chip Architectures in the Nanoscale Era covers the foundations and design methods of network on chip NoC technology The contributors draw on their own lessons learned to provide strong practical guidance on various design issues Exploring the design process of the

Recent Trends in Information and Communication Technology Faisal Saeed, Nadhmi Gazem, Srikanta Patnaik, Ali Saleh Saed Balaid, Fathey Mohammed, 2017-05-24 This book presents 94 papers from the 2nd International Conference of Reliable Information and Communication Technology 2017 IRICT 2017 held in Johor Malaysia on April 23 24 2017 Focusing on the latest ICT innovations for data engineering the book presents several hot research topics including advances in big data analysis techniques and applications mobile networks applications and usability reliable communication systems advances in computer vision artificial intelligence and soft computing reliable health informatics and cloud computing environments e learning acceptance models recent trends in knowledge management and software engineering security issues in the cyber world as well as society and information technology

Designing 2D and 3D

Network-on-Chip Architectures Konstantinos Tatas,Kostas Siozios,Dimitrios Soudris,Axel Jantsch,2013-10-08 This book covers key concepts in the design of 2D and 3D Network on Chip interconnect It highlights design challenges and discusses fundamentals of NoC technology including architectures algorithms and tools Coverage focuses on topology exploration for both 2D and 3D NoCs routing algorithms NoC router design NoC based system integration verification and testing and NoC reliability Case studies are used to illuminate new design methodologies **Networks-on-Chip** Sheng Ma,Libo

Huang,Mingche Lai,Wei Shi,2014-12-04 Networks on Chip From Implementations to Programming Paradigms provides a thorough and bottom up exploration of the whole NoC design space in a coherent and uniform fashion from low level router buffer and topology implementations to routing and flow control schemes to co optimizations of NoC and high level programming paradigms This textbook is intended for an advanced course on computer architecture suitable for graduate students or senior undergrads who want to specialize in the area of computer architecture and Networks on Chip It is also intended for practitioners in the industry in the area of microprocessor design especially the many core processor design with a network on chip Graduates can learn many practical and theoretical lessons from this course and also can be motivated to delve further into the ideas and designs proposed in this book Industrial engineers can refer to this book to make practical tradeoffs as well Graduates and engineers who focus on off chip network design can also refer to this book to achieve deadlock free routing algorithm designs Provides thorough and insightful exploration of NoC design space Description from low level logic implementations to co optimizations of high level program paradigms and NoCs The coherent and uniform format offers readers a clear quick and efficient exploration of NoC design space Covers many novel and exciting research ideas which encourage researchers to further delve into these topics Presents both engineering and theoretical contributions The detailed description of the router buffer and topology implementations comparisons and analysis are of high engineering value **Algorithms and Architectures for Parallel Processing** Guojun Wang,Albert

Zomaya,Gregorio Martinez,Kenli Li,2015-11-16 This four volume set LNCS 9528 9529 9530 and 9531 constitutes the refereed proceedings of the 15th International Conference on Algorithms and Architectures for Parallel Processing ICA3PP 2015 held in Zhangjiajie China in November 2015 The 219 revised full papers presented together with 77 workshop papers in these four volumes were carefully reviewed and selected from 807 submissions 602 full papers and 205 workshop papers The first volume comprises the following topics parallel and distributed architectures distributed and network based computing and internet of things and cyber physical social computing The second volume comprises topics such as big data and its applications and parallel and distributed algorithms The topics of the third volume are applications of parallel and distributed computing and service dependability and security in distributed and parallel systems The covered topics of the fourth volume are software systems and programming models and performance modeling and evaluation **Network and Parallel Computing** Chen Ding,Zhiyuan Shao,Ran Zheng,2010-09-10 This book constitutes the refereed proceedings of the IFIP

International Conference NPC 2010 held in Zhengzhou China in September 2010 The 39 papers presented were carefully selected from 89 submissions The papers are organized in topical sections on Parallelization and Optimization Parallel Algorithms Network CPU and Multicore Cloud and Grid Infrastructure Network on Chip **Efficient Microarchitecture for Network-on-chip Routers** Daniel Ulf Becker, 2012 Continuing advances in semiconductor technology coupled with an increasing concern for energy efficiency have led to an industry wide shift in focus towards modular designs that leverage parallelism in order to meet performance goals Networks on Chip NoCs are widely regarded as a promising approach for addressing the communication challenges associated with future Chip Multi Processors CMPs in the face of further increases in integration density In the present thesis we investigate implementation aspects and design trade offs in the context of routers for NoC applications In particular our focus is on developing efficient control logic for high performance router implementations Using parameterized RTL implementations we first evaluate representative Virtual Channel VC and switch allocator architectures in terms of matching quality delay area and power We also investigate the sensitivity of these properties to key network parameters as well as the impact of allocation on overall network performance Based on the results of this study we propose microarchitectural modifications that improve delay area and energy efficiency Sparse VC allocation reduces the complexity of VC allocators by exploiting restrictions on transitions between packet classes Two improved schemes for speculative switch allocation improve delay and cost while maintaining the critical latency improvements at low to medium load this is achieved by incurring a minimal loss in throughput near the saturation point We also investigate a practical implementation of combined VC and switch allocation and its impact on network cost and performance The second part of the thesis focuses on router input buffer management We explore the design trade offs involved in choosing a buffer organization and we evaluate practical static and dynamic buffer management schemes and their impact on network performance and cost We furthermore show that buffer sharing can lead to severe performance degradation in the presence of congestion To address this problem we introduce Adaptive Backpressure ABP a novel scheme that improves the utilization of dynamically managed router input buffers by varying the stiffness of the flow control feedback loop based on downstream congestion By inhibiting unproductive buffer occupancy this mitigates undesired interference effects between workloads with differing performance characteristics **Proceedings of the 36th Annual IEEE/ACM International Symposium on Microarchitecture** , 2003 MICRO 36 discusses new microarchitecture and software techniques and explores the latest research related to processor architecture compilers and systems for technical interaction on traditional MICRO topics The proceedings also places a special emphasis on optimizations that take advantage of application specific opportunities In addition this year s MICRO includes papers that will benefit both the microarchitecture and embedded architecture communities *Integrated Circuit and System Design* , 2004 **Proceedings of the 2006 International Conference on Supercomputing** , 2006 **Dissertation Abstracts**

International ,2009 **Chip Multiprocessor Coherence and Interconnect System Design** Natalie D. Enright
Jerger,2008 **SBCCI 2006** ,2006 *CODES+ISSS* ,2004 Science Abstracts ,1995 *Hot Interconnects 11* ,2003
Index to IEEE Publications Institute of Electrical and Electronics Engineers,1996 **ACM SIGPLAN notices** ,1991

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