

Manjul Bhushan  
Mark B. Ketchen

# Microelectronic Test Structures for CMOS Technology

# Microelectronic Test Structures For Cmos Technology

**Michael Brown**



## **Microelectronic Test Structures For Cmos Technology:**

**Microelectronic Test Structures for CMOS Technology** Manjul Bhushan, Mark B. Ketchen, 2011-08-26

Microelectronic Test Structures for CMOS Technology and Products addresses the basic concepts of the design of test structures for incorporation within test vehicles scribe lines and CMOS products The role of test structures in the development and monitoring of CMOS technologies and products has become ever more important with the increased cost and complexity of development and manufacturing In this timely volume IBM scientists Manjul Bhushan and Mark Ketchen emphasize high speed characterization techniques for digital CMOS circuit applications and bridging between circuit performance and characteristics of MOSFETs and other circuit elements Detailed examples are presented throughout many of which are equally applicable to other microelectronic technologies as well The authors overarching goal is to provide students and technology practitioners alike a practical guide to the disciplined design and use of test structures that give unambiguous information on the parametrics and performance of digital CMOS technology *CMOS Test and Evaluation* Manjul Bhushan, Mark B. Ketchen, 2014-12-03 CMOS Test and Evaluation A Physical Perspective is a single source for an integrated view of test and data analysis methodology for CMOS products covering circuit sensitivities to MOSFET characteristics impact of silicon technology process variability applications of embedded test structures and sensors product yield and reliability over the lifetime of the product This book also covers statistical data analysis and visualization techniques test equipment and CMOS product specifications and examines product behavior over its full voltage temperature and frequency range [Proceedings of the ... IEEE International Conference on Microelectronic Test Structures](#), 1988

[Latchup](#) Steven H. Voldman, 2008-04-15 Interest in latchup is being renewed with the evolution of complimentary metal oxide semiconductor CMOS technology metal oxide semiconductor field effect transistor MOSFET scaling and high level system on chip SOC integration Clear methodologies that grant protection from latchup with insight into the physics technology and circuit issues involved are in increasing demand This book describes CMOS and BiCMOS semiconductor technology and their sensitivity to present day latchup phenomena from basic over voltage and over current conditions single event latchup SEL and cable discharge events CDE to latchup domino phenomena It contains chapters focusing on bipolar physics latchup theory latchup and guard ring characterization structures characterization testing product level test systems product level testing and experimental results Discussions on state of the art semiconductor processes design layout and circuit level and system level latchup solutions are also included as well as latchup semiconductor process solutions for both CMOS to BiCMOS such as shallow trench deep trench retrograde wells connecting implants sub collectors heavily doped buried layers and buried grids from single to triple well CMOS practical latchup design methods automated and bench level latchup testing methods and techniques latchup theory of logarithm resistance space generalized alpha a space beta b space new latchup design methods connecting the theoretical to the practical analysis and examples of latchup computer aided

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