

The Role of the Original PCI Solution

Don't Throw Away What is Good! Keep It

The PCI Express architects have carried forward the most beneficial features from previous generation bus architectures and have also taken advantages of new developments in computer architecture.

For example, PCI Express employs the same usage model and load-store communication model as PCI and PCI-X. PCI Express supports familiar transactions such as memory read/write, IO read/write and configuration read/write transactions. The memory, IO and configuration address space model is the same as PCI and PCI-X address spaces. By maintaining the address space model, existing OSs and driver software will run in a PCI Express system without any modifications. In other words, PCI Express is software backwards compatible with PCI and PCI-X systems. In fact, a PCI Express system will boot an existing OS with no changes to current drivers and application programs. Even PCI/ACPI power management software will still run.

Like predecessor buses, PCI Express supports chip-to-chip interconnect and board-to-board interconnect via cards and connectors. The connector and card structure are similar to PCI and PCI-X connectors and cards. A PCI Express motherboard will have a similar form factor to existing FR4 ATX motherboards which is encased in the familiar PC package.

Make Improvements for the Future

To improve bus performance, reduce overall system cost and take advantage of new developments in computer design, the PCI Express architecture had to be significantly re-designed from its predecessor buses. PCI and PCI-X buses are multi-drop parallel interconnect buses in which many devices share one bus.

PCI Express on the other hand implements a serial, point-to-point type interconnect for communication between two devices. Multiple PCI Express devices are interconnected via the use of switches which means one can practically connect a large number of devices together in a system. A point-to-point interconnect implies limited electrical load on the link allowing transmission and reception frequencies to scale to much higher numbers. Currently PCI Express transmission and reception data rate is 2.5 Gbits/sec. A serial interconnect between two devices results in fewer pins per device package which reduces PCI Express chip and board design cost and reduces board design complexity. PCI Express performance is also highly scalable. This is achieved by implement-

Pci Express System Architecture

Pci Express System Architecture

Sam Siewert

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PCI Express System Architecture Ravi Budruk,Don Anderson,Tom Shanley,2004 PCI EXPRESS is considered to be the most general purpose bus so it should appeal to a wide audience in this arena Today s buses are becoming more specialized to meet the needs of the particular system applications building the need for this book Mindshare and their only competitor in this space Solari team up in this new book

PCI Express System Architecture Ravi Budruk Don Anderson (MindShare, Inc, Tom Shanley),2003 80486 System Architecture Tom Shanley,MindShare, Inc,1995 80486 System Architecture describes the hardware architecture of PC products using the Intel family of 80486 chips providing a clear concise explanation of the 80486 processor s relationship to the rest of the system The author provides a comprehensive treatment of the processor including 80486 microarchitecture and its functional units internal and external caches hardware interface SL technology features instructions new to the 80486 the register set 486 487SX processors 486DX2 processors 486DX2 write back enhanced processor 486DX4 processors implementation specific issues main memory subsystem design OverDrive processors If you design or test hardware or software that involves 486 processors 80486 System Architecture is an essential time saving tool The PC System Architecture Series is a crisply written and comprehensive set of guides to the most important PC hardware standards Each title explains from a programmer s perspective the architecture features and operations of systems built using one particular type of chip or hardware specification The PC System Architecture Series features step by step descriptions and instructions and accessible illustrations that enable a wide range of readers to easily understand difficult hardware topics The authors expert hardware training consultants for clients including IBM Intel Compaq and Dell have mastered the art of pinpointing and succinctly explaining just the critical information that PC programmers software and hardware designers and engineers need to know and leaving out the rest The result is an exciting series of books that will enable readers of a wide range of backgrounds to make immediate gains in programming productivity

PCI System Architecture Don Anderson,Tom Shanley,MindShare, Inc,1999 Learn all you need to know to engineer reliable high performance PCI products with text written in practical and comprehensive prose The bestselling PCI book for computer engineers now fully updated for PCI Revision 2.2 **Encyclopedia of Parallel Computing** David Padua,2011-09-08 Containing over 300 entries in an A Z format the Encyclopedia of Parallel Computing provides easy intuitive access to relevant information for professionals and researchers seeking access to any aspect within the broad field of parallel computing Topics for this comprehensive reference were selected written and peer reviewed by an international pool of distinguished researchers in the field The Encyclopedia is broad in scope covering machine organization programming languages algorithms and applications Within each area concepts designs and specific implementations are presented The highly structured essays in this work comprise synonyms a definition and discussion of the topic bibliographies and links to related literature Extensive cross references to other entries within the Encyclopedia support

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Introduction to PCI Express Adam H. Wilen,Justin P. Schade,Ron Thornburg,2003 Offering an overview this guide details how 3GIO allows designers to overcome the practical performance limits of existing multidrop parallel bus technology and

explains how to increase performance and new capabilities for a broad range of computing and communications platforms

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