

Formal Verification of Superscalar Microprocessors with Multicycle Functional Units, Exceptions, and Branch Prediction¹

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Abstract

We extend the Burch and Dill flushing technique [6] for formal verification of microprocessors to be applicable to designs where the functional units and memories have multicycle and possibly arbitrary latency. We also show ways to incorporate exceptions and branch prediction by exploiting the properties of the logic of Positive Equality with Uninterpreted Functions [4][5]. We study the modeling of the above features in different versions of dual-issue superscalar processors.

1 Introduction

In order for formal methods to scale for verification of modern microprocessors, they need to be applicable easily and with a high degree of automation to designs with multicycle functional units, multicycle memories, exceptions, and branch prediction. Burch and Dill's verification methodology has the potential to be highly automatic, but has previously been applied only to designs with single-cycle functional units and memories that produce their results instantaneously [5][6][7][21]. The approach is very elegant in using *flushing* of the processor—feeding it with bubbles until all instructions in flight complete their execution—in order to compute an abstraction function mapping Implementation states to a Specification state. (The difference between a bubble and a nop is that a bubble does not modify any user-visible state, while a nop increments the PC.) The correctness criterion is a commutative diagram, stating that an application of the transition function of the Implementation followed by flushing should produce the same user-visible state as first flushing the Implementation and then using the resultant user-visible state to apply the transition function of the Specification between 0 and k times, where k is the issue-width of the Implementation. As observed and exploited by Burch in his controlled flushing [7], we can change the logic during flushing, since the only purpose of that logic is to compute an abstraction function. Having an improper abstraction function will not compromise the verification and can only result in a false negative.

The same correctness criterion has been adopted by the theorem-proving community and applied to an out-of-order design with exceptions and interrupts by Sawada and Hunt [17] and to an out-of-order design with only arithmetic instructions by

Hosabettu, Srivas and Gopalakrishnan [13]. However, the former approach requires the user to manually build an intermediate abstraction of the processor and to define a large number of lemmas (Sawada defined nearly 4,000), necessary for the correctness proof. The latter approach requires the user to manually define a set of completion functions, one per unfinished instruction in flight, describing how that instruction will be completed, given that all the instructions that it has data dependencies on have already been completed. Furthermore, the user has to manually define a way to compose these completion functions in order to form the abstraction function for the processor. Both of these theorem-proving methods require months of manual work for complex designs, i.e., they are not automatic.

Not only has the Burch and Dill flushing technique not been applied to processors with multicycle functional units, but Hosabettu, Srivas and Gopalakrishnan [12] have claimed that it has the drawback of being hard to use for pipelines with indeterminate latency, particularly where an ALU computation might have a data-dependent duration or a memory hierarchy of multiple levels might have a non-deterministic delay.

In this work we extend Burch and Dill's flushing-based methodology to be applicable to microprocessors with functional units and memories of multicycle and possibly arbitrary latency. We also model exceptions and branch prediction. Our most complex designs have 10 abstract instruction types. They have two completely functional pipelines, each consisting of five stages, for a total of up to 10 instructions in flight. Therefore, exhaustive binary simulation must consider 10^{10} instruction sequences of 10 instructions each. Furthermore, accounting for possible data dependencies, raised exceptions, correctness/incorrectness of the branch predictions, and multicycle computations will make that number significantly higher. Even directed simulation will probably find it very hard, if at all possible, to generate all interesting instruction sequences for such a design. However, we were able to formally verify it in less than 44 minutes of CPU time.

2 Background

The key to our success is a very efficient decision procedure [21] for the logic of Equality with Uninterpreted Functions and Memories (EUFM) [6], which exploits the properties of Positive Equality [4][5] and the e_v encoding [10] to generate a propositional formula, which is then evaluated with BDDs [3] or SAT-checkers. We found BDDs to be unmatched by SAT-checkers and SVC [18] (a decision procedure for the logic of EUFM that does not exploit Positive Equality) when verifying correct designs. However, SAT-checkers outperform BDDs on buggy processors.

The syntax of EUFM [6] includes terms and formulas. A term can be an Uninterpreted Function (UF) applied on a list of argument terms, a domain variable, or an *ITE* operator selecting between two argument terms based on a controlling formula, such that *ITE(formula, term1, term2)* will evaluate to *term1* when *formula* = **true** and to *term2* when *formula* = **false**. A formula can be an Uninterpreted Predicate (UP) applied on a list of argu-

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Book Formal Verification Microprocessors Automatic Superscalar

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Kulkarni, E. Brockmeyer, Per Gunnar
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Formal Verification of Microprocessors Miroslav Velez, 2015-02-04 Formal verification is the mathematical proof of correctness of computer systems Microprocessors are the most important components in computer systems and are increasingly being used in safety critical applications e.g. to monitor the health of patients to control the engines and breaks of cars to drive autonomous vehicles and fly autonomous aircraft and to control weapons systems As such the correctness of microprocessors is a matter of public safety and national security Furthermore for the companies that design and manufacture microprocessors or systems controlled by them the correctness of microprocessors is a matter of business success or failure Statistics from industrial microprocessor designs indicate that up to 90% of the engineering effort is spent on verification which increasingly becomes the bottleneck in developing new products Formal verification has the potential to significantly reduce the design time while also guaranteeing complete correctness However previous approaches for formal verification of microprocessors either do not scale for complex designs or require prohibitive amounts of manual effort by experts In contrast this book presents a highly automatic and scalable method for formal verification of complex processors including pipelined superscalar and VLIW designs

Memory, Microprocessor, and ASIC Wai-Kai Chen, 2003-03-26 Timing memory power dissipation testing and testability are all crucial elements of VLSI circuit design In this volume culled from the popular VLSI Handbook experts from around the world provide in depth discussions on these and related topics Stacked gate embedded and flash memory all receive detailed treatment including their power cons

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Design of Systems on a Chip: Design and Test Ricardo Reis, Marcelo Soares Lubaszewski, Jochen A.G. Jess, 2007-05-06 This book is the second of two volumes addressing the design challenges associated with new generations of semiconductor technology The various chapters are compiled from tutorials presented at workshops in recent years by prominent authors from all over the world Technology productivity and quality are the main aspects under consideration to establish the major requirements for the design and test of upcoming systems on a chip

Proceedings of the ASP-DAC ... Asia and South Pacific Design Automation Conference ,1995

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Microprocessor 4 Philippe Darche, 2021-02-17 Since its commercialization in 1971 the microprocessor a modern and integrated form of the central processing unit has continuously broken records in terms of its integrated functions computing power low costs and energy saving status Today it is present in almost all electronic devices Sound knowledge of its internal mechanisms and programming is essential for electronics and computer engineers to understand and master computer operations and advanced programming concepts This book in five volumes focuses more particularly on the first two generations of microprocessors those that handle 4 and 8 bit integers Microprocessor 4 the fourth of five volumes addresses the software aspects of this component Coding of an instruction addressing modes and the main features of the Instruction Set Architecture ISA of a generic component are presented Furthermore two approaches are discussed for altering the flow of execution using mechanisms of subprogram and interrupt A comprehensive approach is used with examples drawn from

current and past technologies that illustrate theoretical concepts making them accessible Data Access and Storage Management for Embedded Programmable Processors Francky Catthoor, K. Danckaert, K.K. Kulkarni, E. Brockmeyer, Per Gunnar Kjeldsberg, T. van Achteren, Thierry Omnes, 2013-03-14 Data Access and Storage Management for Embedded Programmable Processors gives an overview of the state of the art in system level data access and storage management for embedded programmable processors The targeted application domain covers complex embedded real time multi media and communication applications Many of these applications are data dominated in the sense that their cost related aspects namely power consumption and footprint are heavily influenced if not dominated by the data access and storage aspects The material is mainly based on research at IMEC in this area in the period 1996 2001 In order to deal with the stringent timing requirements and the data dominated characteristics of this domain we have adopted a target architecture style that is compatible with modern embedded processors and we have developed a systematic step wise methodology to make the exploration and optimization of such applications feasible in a source to source precompilation approach **A Framework for the Specification, Design, and Verification of Pipelines with Structural Hazards** Mark Aagaard, 1995 Science Abstracts ,1993 **Proceedings** ,1995 *Computer & Control Abstracts* ,1996 **A Systematic Methodology for Verifying Superscalar Microprocessors** Mandayam Srivas, 1999 The Indispensable Pentium Book Hans-Peter Messmer, 1995 Providing a unique comparison with competing RISC implementations The Indispensable Pentium Book offers a comprehensive treatment of this important processor for all PC programmers *American Book Publishing Record* ,1991 *Advanced Backend Code Optimization* Sid Touati, Benoit Dupont de Dinechin, 2014-06-02 This book is a summary of more than a decade of research in the area of backend optimization It contains the latest fundamental research results in this field While existing books are often more oriented toward Masters students this book is aimed more towards professors and researchers as it contains more advanced subjects It is unique in the sense that it contains information that has not previously been covered by other books in the field with chapters on phase ordering in optimizing compilation register saturation in instruction level parallelism code size reduction for software pipelining memory hierarchy effects and instruction level parallelism Other chapters provide the latest research results in well known topics such as register need and software pipelining and periodic register allocation **Cornell University Courses of Study** Cornell University, 2006 *XIII SBMicro, International Conference on Microelectronics and Packaging, ICMP'98: Advanced courses and invited papers* Ivan Jorge Chueiri, Carlos Alberto dos Reis Filho, 1998 **Index to IEEE Publications** Institute of Electrical and Electronics Engineers, 1995

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