

High speed serial link design (SERDES)

Introduction, Architectures and applications

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Abstract This paper describes basic methods of transferring data through serial data buses, using serializer-deserializer (SerDes) as main device in this operation. It explains function of SerDes and different techniques for implementing it.

Keywords: SERDES, Clock and data recovery, High speed SerDes, Parallel clock SERDES, Embedded clock SERDES, Shared SERDES, Bit interleaving SERDES

I. INTRODUCTION

The simplest method of transferring data through the inputs or outputs of a silicon chip is to directly connect the datapath from one chip to the next chip. Since data often consist of more than one bit of information, the datapath is more than one-bit wide.

There are two inherent problems of the parallel data bus. The first problem is that n input/output (I/O) pins are required on each chip to transfer the data. The second problem involves meeting timing requirements. Due to these two problems we thought about transforming parallel data to serial streams of data to be able to use serial communications off-chips and on-chips.

Serializers/Deserializers (SerDes) are the main devices which convert parallel data into stream of serial data and send it through a channel.

Serial interconnects form the critical backbone of modern communication systems, so the choice of SerDes can have a big impact on system cost and performance. While the range of choices may seem confusing at first, SerDes devices fall into a few basic architectures, each tailored to specific application requirements. A basic understanding of these architectural differences enables the designer to quickly find the right SerDes for the application. In this paper we examine four distinct SerDes architectures and show how each plays a vital role in today's systems.

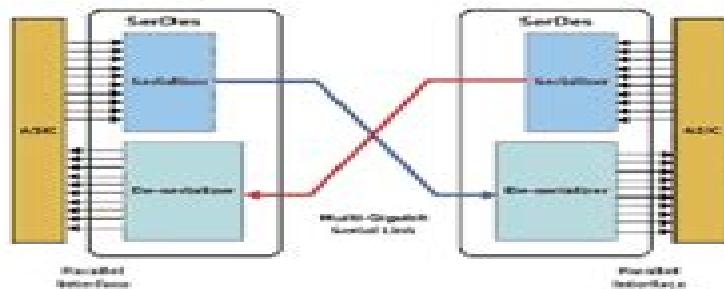


Fig. 1 serial-to-parallel device

II. ARCHITECTURE OF HIGH-SPEED SERDES

High-speed Serializer/Deserializer (HSS) devices are the dominant implementation of I/O interfaces at speed of 2.5 Gbps and higher. Such devices are differentiated from source-synchronous interface in that the receiver device contains a clock data recovery (CDR) circuit dynamically determines the optimal sampling point of the data signal based upon the transition edges of the signal. In other words clock information is extracted directly from the data rather than relying on a separate clock.



Fig. 2 HSS basic block diagram

Fig. 2 illustrate the basic block diagram of the transmit and receive channels of an HSS device. The transmitter serializes parallel data, equalizes it and then drives the serial data onto a differential signal pair of interconnect wires. The receiver consists of a differential receiver, a CDR circuit which may also integrate an equalizer and deserializes the data upon the sample point established by the CDR.

SerDes cores which contain only transmit or only receive channels are called **simplex cores**; SerDes cores which contain both transmit and receive channels are called **full duplex cores**. Note that the terminology "full duplex" does not imply that the electrical interface is bidirectional. Any given electrical interconnect channel has a fixed direction of data transmission. If a protocol application requires "full duplex" communication, then independent transmit and receive channels with independent interconnections are used to implement the interface.



Simplex core, no Rx clock



Half-Duplex core, Rx has Rx clock



Full-Duplex core, Rx has Rx clock

Fig. 3 different types of serdes cores

Book High Speed Serial Link Measurement

Jane Holcombe,Charles Holcombe

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High Speed Serial Link Moises Cases, Bhyrav Mutnury, 2025-07-08 This book focuses on the high speed serial HSS system design as it relates to electronic system design engineers, electronic packaging engineers, and to signal and power integrity engineers. The book covers basic concepts, input output I/O signalling, including trends, protocols, basic signal and power integrity concepts, an overview of current HSS system design and specifications, channel loss components, typical HSS topologies, electrical modelling methodology and techniques, link simulation techniques, link analysis and optimization, and link measurement parameters and techniques. It includes practical design examples and recommendations, as well as typical measurement parameter values and failure analysis.

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Data Communications Data Book, 1996 **Digital**

Communications Test and Measurement Dennis Derickson, Marcus Müller, 2007-12-10 A Comprehensive Guide to Physical Layer Test and Measurement of Digital Communication Links. Today's new data communication and computer interconnection systems run at unprecedented speeds, presenting new challenges not only in the design but also in troubleshooting, test and measurement. This book assembles contributions from practitioners at top test and measurement companies, component manufacturers and universities. It brings together information that has never been broadly accessible before, information that was previously buried in application notes, seminar and conference presentations, short courses and unpublished works. Readers will gain a thorough understanding of the inner workings of digital high speed systems and learn how the different aspects of such systems can be tested. The editors and contributors cover key areas in test and measurement of transmitters, digital waveform and jitter analysis, and bit error ratio receivers, sensitivity, jitter tolerance and PLL CDR characterization, and high speed channel characterization in time and frequency domain. Extensive illustrations are provided throughout. Coverage includes Signal integrity from a measurement point of view, Digital waveform analysis using high bandwidth real time and sampling equivalent time oscilloscopes, Bit error ratio measurements for both electrical and optical links, Extensive coverage on the topic of jitter in high speed networks, State of the art optical sampling techniques for analysis of 100 Gbit/s signals, Receiver characterization, clock recovery, phase locked loops, jitter tolerance and transfer.

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