Design and Verification of AHB Protocol Using System Verilog and Universal Verification Methodology (UVM)

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ABSTRACT :
Recently, VLSI technology has improved significantly and more transistors can be incorporated in a chip. A System on-Chip (SOC) Configuration have number of blocks are integrated on a single chip. Numerous blocks are integrated in single IC, but to access their function, they requires a powerful communication architecture. This can only be achieved by using on–chip bus architecture to meet their requirements. Different Companies has various on-Chip Bus architectures but one of the most suitable architecture is AMBA by ARM. AMBA consist of three buses, namely, Advanced Systems Bus (ASB), Advanced Peripheral Bus (APB) and Advanced High Performance Bus (AHB), when compared to other two buses AHB is high performance, high bandwidth and for high clock frequency system modules the System designers select AHB as their primary choice. The AHB (Advanced High-performance Bus) is a superior bus in AMBA (Advanced Microcontroller Bus Architecture) family. It is a norm for intercommunication of modules in a framework. The AHB (Advance High performance) bus Standards are characterized by ARM which supports for the communication of on–chip memories, processors and interfaces of external off-chip memory. Here the basic blocks such as master, slave, decoder, and arbiter are used to design and verify an AHB that supports multiples master and multiples slave. The conventional way of verification is simulation based. As the Technology improves the complexity of IC's has been increased. Thus, time spent on verification has also been increased. The main focus is to design of AHB protocol in Verilog and verify using Hardware verification language such as System Verilog and standard Methodology such as Universal Verification Methodology (UVM). QuestaSim (Advanced verification tool from Mentor Graphics) is an EDA tool used to simulate and verify the design and obtain Coverage report.
Keywords — AMBA, AHB, APB, ASB, OCB, SOC, UVM

I. INTRODUCTION

1.1 About AMBA bus

The AMBA is an Advanced Microcontroller Bus Architecture defined by ARM, it is an open standard widely used for an on-chip bus system. The standard is intends to simplify the component design by allowing the use of interchangeable parts the within the SoC style. It promotes the use of holding parts, so that a minimum of a neighborhood of the SoC can be reconstructed, instead of having to rewrite it entirely each time. AHB (Advanced High-performance Bus), ASB (Advanced System Bus), and APB (Advanced Peripheral Bus) are the bus groups defined in the AMBA. AHB. The AHB is employed for high-performance, high frequency architecture. These applications includes are ARM cores and high-speed RAM inside the system, Nand Flash, DMA and Bridge links. [1] The APB is used for connecting external devices such as UART, keypad and timer, and has low performance requirements, while it is used for optimizing power consumption. AMBA is the Standard bus-based microcontroller typical feature a high-performance system hub bus (AHB or ASB) that supports for external memory bandwidth, including CPUs, on–chip memories, and other direct data access (DMA) devices. For most of the transmission between various units, such as CPUs, on-chip memories, and DMA, the bus serves as a high bandwidth interface.

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ASIC/SoC Functional Design Verification Ashok B. Mehta,2017-06-28 This book describes in detail all required technologies and methodologies needed to create a comprehensive functional design verification strategy and environment to tackle the toughest job of guaranteeing first pass working silicon The author first outlines all of the verification sub fields at a high level with just enough depth to allow an engineer to grasp the field before delving into its detail He then describes in detail industry standard technologies such as UVM Universal Verification Methodology SVA SystemVerilog Assertions SFC SystemVerilog Functional Coverage CDV Coverage Driven Verification Low Power Verification Unified Power Format UPF AMS Analog Mixed Signal verification Virtual Platform TLM2 0 ESL Electronic System Level methodology Static Formal Verification Logic Equivalency Check LEC Hardware Acceleration Hardware Emulation Hardware Software Co verification Power Performance Area PPA analysis on a virtual platform Reuse Methodology from Algorithm ESL to RTL and other overall methodologies **SystemVerilog for Design and Verification using UVM** Mark A. Azadpour,2015-02-04 This book is an A Z guide to using SystemVerilog for ASIC design from conception to RTL coding to synthesis and verification Readers will benefit from a thorough introduction to the powerful constructs and features of SystemVerilog In addition the verification methodology of Universal Verification Methodology UVM is used to build test benches that allow for verification of complicated designs and synthesis basics are discussed using the Synopsys Design Compiler DC To complete this book s package as a practical guide readers are introduced to the fundamentals of static timing analysis IP Cores Design from Specifications to Production Khaled Salah Mohamed,2015-08-27 This book describes the life cycle process of IP cores from specification to production including IP modeling verification optimization and protection Various trade offs in the design process are discussed including those associated with many of the most common memory cores controller IPs and system on chip SoC buses Readers will also benefit from the author s practical coverage of new verification methodologies such as bug localization UVM and scan chain A SoC case study is presented to compare traditional verification with the new verification methodologies Discusses the entire life cycle process of IP cores from specification to production including IP modeling verification optimization and protection Introduce a deep introduction for Verilog for both implementation and verification point of view Demonstrates how to use IP in applications such as memory controllers and SoC buses Describes a new verification methodology called bug localization Presents a novel scan chain methodology for RTL debugging Enables readers to employ UVM methodology in straightforward practical terms Advances in Computing and Network Communications Sabu M. Thampi,Erol Gelenbe,Mohammed Atiquzzaman,Vipin Chaudhary,Kuan-Ching Li,2021-04-20 This book constitutes the thoroughly refereed post conference proceedings of the 4th International Conference on Computing and Network Communications CoCoNet 20 October 14 17 2020 Chennai India The papers presented were carefully reviewed and selected from several initial submissions The papers are organized in topical sections on Signal Image and Speech Processing

Wireless and Mobile Communication Internet of Things Cloud and Edge Computing Distributed Systems Machine Intelligence Data Analytics Cybersecurity Artificial Intelligence and Cognitive Computing and Circuits and Systems The book is directed to the researchers and scientists engaged in various fields of computing and network communication domains   Advances in VLSI and Embedded Systems Zuber Patel,Shilpi Gupta,Nithin Kumar Y. B.,2020-08-28 This book presents select peer reviewed proceedings of the International Conference on Advances in VLSI and Embedded Systems AVES 2019 held at SVNIT Surat Gujarat India The book covers cutting edge original research in VLSI design devices and emerging technologies embedded systems and CAD for VLSI With an aim to address the demand for complex and high functionality systems as well as portable consumer electronics the contents focus on basic concepts of circuit and systems design fabrication testing and standardization This book can be useful for students researchers as well as industry professionals interested in emerging trends in VLSI and embedded systems   Computer Networks and Inventive Communication Technologies S. Smys,Ram Palanisamy,Álvaro Rocha,Grigorios N. Beligiannis,2021-06-02 This book is a collection of peer reviewed best selected research papers presented at 3rd International Conference on Computer Networks and Inventive Communication Technologies ICCNCT 2020 The book covers new results in theory methodology and applications of computer networks and data communications It includes original papers on computer networks network protocols and wireless networks data communication technologies and network security The proceedings of this conference is a valuable resource dealing with both the important core and the specialized issues in the areas of next generation wireless network design control and management as well as in the areas of protection assurance and trust in information security practice It is a reference for researchers instructors students scientists engineers managers and industry practitioners for advance work in the area   *Information and Communication Technology for Competitive Strategies* Simon Fong,Shyam Akashe,Parikshit N. Mahalle,2018-08-30 This book contains 74 papers presented at ICTCS 2017 Third International Conference on Information and Communication Technology for Competitive Strategies The conference was held during 16 17 December 2017 Udaipur India and organized by Association of Computing Machinery Udaipur Professional Chapter in association with The Institution of Engineers India Udaipur Local Center and Global Knowledge Research Foundation This book contains papers mainly focused on ICT for Computation Algorithms and Data Analytics and IT Security etc   **VLSI Design Methodology Development** Thomas Dillinger,2019-06-17 The Complete Modern Tutorial on Practical VLSI Chip Design Validation and Analysis As microelectronics engineers design complex chips using existing circuit libraries they must ensure correct logical physical and electrical properties and prepare for reliable foundry fabrication VLSI Design Methodology Development focuses on the design and analysis steps needed to perform these tasks and successfully complete a modern chip design Microprocessor design authority Tom Dillinger carefully introduces core concepts and then guides engineers through modeling functional design validation design implementation electrical analysis and release to manufacturing Writing from

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Verification Methodology *SystemVerilog Assertions Handbook, 4th Edition* Ben Cohen,Srinivasan Venkataramanan,Lisa Piper,Ajeetha Kumari,2015-10-15 SystemVerilog Assertions Handbook 4th Edition is a follow up book to the popular and highly recommended third edition published in 2013 This 4th Edition is updated to include 1 A new section on testbenching assertions including the use of constrained randomization along with an explanation of how constraints operate and with a definition of the most commonly used constraints for verifying assertions 2 More assertion examples and comments that were derived from users experiences and difficulties in using assertions many of these issues were reported in newsgroups such as the verificationAcademy com and the verificationGuild com 3 Links to new papers on the use of assertions such as in a UVM environment 4 Expected updates on assertions in the upcoming IEEE 1800 2018 Standard for SystemVerilog Unified Hardware Design Specification and Verification Language The SVA goals for this 1800 2018 were to maintain stability and not introduce substantial new features However a few minor enhancements were identified and are expected to be approved The 3rd Edition of this book was based on the IEEE 1800 2012 **A Practical Guide to Adopting the Universal Verification Methodology (UVM) Second Edition** Hannibal Height,2012-12-18 With both cookbook style examples and in depth verification background novice and expert verification engineers will find information to ease their adoption of this emerging Accellera standard **SystemVerilog Assertions Handbook** Ben Cohen,Srinivasan Venkataramanan,Ajeetha Kumari,2005 *Practical Uvm* Srivatsa Vasudevan,2016-07-20 The Universal Verification Methodology is an industry standard used by many companies for verifying ASIC devices In this book you will find step by step instructions coding guidelines and debugging features of UVM explained clearly using examples The book also covers the changes from UVM 1 1d to UVM 1 2 and provides details of the enhancements in the upcoming IEEE 1800 2 UVM standard http www accellera org community uvm faq The Table of Contents Preface Foreword from UVM committee members and detailed information on this book is available on www uvmbook com **A Practical Guide to Adopting the Universal Verification Methodology (UVM)** Sharon Rosenberg,Kathleen A. Meade,2010 Advanced Verification Topics Bishnupriya Bhattacharya,John Decker,Gary Hall,Nick Heaton,Yaron Kashai,Neyaz Khan,Zeev Kirshenbaum,Efrat Shneydor,2011-09-30 The Accellera Universal Verification Methodology UVM standard is architected to scale but verification is growing and in more than just the digital design dimension It is growing in the SoC dimension to include low power and mixed signal and the system integration dimension to include multi language support and acceleration These items and others all contribute to the quality of the SOC so the Metric Driven Verification MDV methodology is needed to unify it all into a coherent verification plan This book is for verification engineers and managers familiar with the UVM and the benefits it brings to digital verification but who also need to tackle specialized tasks It is also written for the SoC project manager that is tasked with building an efficient worldwide team While the task continues to become more complex Advanced Verification Topics describes methodologies outside of the Accellera UVM standard but that build on it to provide a way for SoC teams to stay productive

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