

Manjul Bhushan  
Mark B. Ketchen

# Microelectronic Test Structures for CMOS Technology

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**SA Adler**



## **Microelectronic Test Structures For Cmos Technology:**

**Microelectronic Test Structures for CMOS Technology** Manjul Bhushan, Mark B. Ketchen, 2011-08-26

Microelectronic Test Structures for CMOS Technology and Products addresses the basic concepts of the design of test structures for incorporation within test vehicles scribe lines and CMOS products The role of test structures in the development and monitoring of CMOS technologies and products has become ever more important with the increased cost and complexity of development and manufacturing In this timely volume IBM scientists Manjul Bhushan and Mark Ketchen emphasize high speed characterization techniques for digital CMOS circuit applications and bridging between circuit performance and characteristics of MOSFETs and other circuit elements Detailed examples are presented throughout many of which are equally applicable to other microelectronic technologies as well The authors overarching goal is to provide students and technology practitioners alike a practical guide to the disciplined design and use of test structures that give unambiguous information on the parametrics and performance of digital CMOS technology CMOS Test and Evaluation Manjul Bhushan, Mark B. Ketchen, 2014-12-03 CMOS Test and Evaluation A Physical Perspective is a single source for an integrated view of test and data analysis methodology for CMOS products covering circuit sensitivities to MOSFET characteristics impact of silicon technology process variability applications of embedded test structures and sensors product yield and reliability over the lifetime of the product This book also covers statistical data analysis and visualization techniques test equipment and CMOS product specifications and examines product behavior over its full voltage temperature and frequency range *Proceedings of the ... IEEE International Conference on Microelectronic Test Structures*, 1988

*Latchup* Steven H. Voldman, 2008-04-15 Interest in latchup is being renewed with the evolution of complimentary metal oxide semiconductor CMOS technology metal oxide semiconductor field effect transistor MOSFET scaling and high level system on chip SOC integration Clear methodologies that grant protection from latchup with insight into the physics technology and circuit issues involved are in increasing demand This book describes CMOS and BiCMOS semiconductor technology and their sensitivity to present day latchup phenomena from basic over voltage and over current conditions single event latchup SEL and cable discharge events CDE to latchup domino phenomena It contains chapters focusing on bipolar physics latchup theory latchup and guard ring characterization structures characterization testing product level test systems product level testing and experimental results Discussions on state of the art semiconductor processes design layout and circuit level and system level latchup solutions are also included as well as latchup semiconductor process solutions for both CMOS to BiCMOS such as shallow trench deep trench retrograde wells connecting implants sub collectors heavily doped buried layers and buried grids from single to triple well CMOS practical latchup design methods automated and bench level latchup testing methods and techniques latchup theory of logarithm resistance space generalized alpha a space beta b space new latchup design methods connecting the theoretical to the practical analysis and examples of latchup computer aided

design CAD methodologies from design rule checking DRC and logical to physical design to new latchup CAD methodologies that address latchup for internal and external latchup on a local as well as global design level Latchup acts as a companion text to the author's series of books on ESD electrostatic discharge protection serving as an invaluable reference for the professional semiconductor chip and system level ESD engineer Semiconductor device process and circuit designers and quality reliability and failure analysis engineers will find it informative on the issues that confront modern CMOS technology Practitioners in the automotive and aerospace industries will also find it useful In addition its academic treatment will appeal to both senior and graduate students with interests in semiconductor process device physics computer aided design and design integration     *Microelectronic Device Technology* ,1999     *1997 IEEE International Conference on Microelectronic Test Structures Proceedings* IEEE Electron Devices Society,1997     **Analog-to-Digital Conversion** Marcel J.M. Pelgrom,2022-03-15 This textbook is appropriate for use in graduate level curricula in analog to digital conversion as well as for practicing engineers in need of a state of the art reference on data converters It discusses various analog to digital conversion principles including sampling quantization reference generation Nyquist architectures and sigma delta modulation This book presents an overview of the state of the art in this field and focuses on issues of optimizing accuracy and speed while reducing the power level This new fourth edition emphasizes novel calibration concepts the specific requirements of systems the consequences of advanced technology and the need for a more statistical approach to accuracy Pedagogical enhancements to this edition include additional new exercises solved examples to introduce all key new concepts and warnings remarks and hints from a practitioner's perspective wherever appropriate Considerable background information and practical tips from designing a PCB to lay out aspects to trade offs on system level complement the discussion of basic principles making this book a valuable reference for the experienced engineer     *ESD* Steven H. Voldman,2011-04-04 Electrostatic discharge ESD continues to impact semiconductor components and systems as technologies scale from micro to nano electronics This book studies electrical overstress ESD and latchup from a whole chip ESD design synthesis approach It provides a clear insight into the integration of ESD protection networks from a generalist perspective followed by examples in specific technologies circuits and chips Uniquely both the semiconductor chip integration issues and floorplanning of ESD networks are covered from a top down design approach Look inside for extensive coverage on integration of cores power bussing and signal pins in DRAM SRAM CMOS image processing chips microprocessors analog products RF components and how the integration influences ESD design and integration architecturing of mixed voltage mixed signal to RF design for ESD analysis floorplanning for peripheral and core I/O designs and the implications on ESD and latchup guard ring integration for both a bottom up and top down methodology addressing I/O guard rings ESD guard rings I/O to I/O and I/O to core classification of ESD power clamps and ESD signal pin circuitry and how to make the correct choice for a given semiconductor chip examples of ESD design for the state of the art technologies

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## **Table of Contents Microelectronic Test Structures For Cmos Technology**

1. Understanding the eBook Microelectronic Test Structures For Cmos Technology
  - The Rise of Digital Reading Microelectronic Test Structures For Cmos Technology
  - Advantages of eBooks Over Traditional Books
2. Identifying Microelectronic Test Structures For Cmos Technology
  - Exploring Different Genres
  - Considering Fiction vs. Non-Fiction
  - Determining Your Reading Goals
3. Choosing the Right eBook Platform
  - Popular eBook Platforms
  - Features to Look for in an Microelectronic Test Structures For Cmos Technology
  - User-Friendly Interface
4. Exploring eBook Recommendations from Microelectronic Test Structures For Cmos Technology
  - Personalized Recommendations
  - Microelectronic Test Structures For Cmos Technology User Reviews and Ratings
  - Microelectronic Test Structures For Cmos Technology and Bestseller Lists
5. Accessing Microelectronic Test Structures For Cmos Technology Free and Paid eBooks
  - Microelectronic Test Structures For Cmos Technology Public Domain eBooks
  - Microelectronic Test Structures For Cmos Technology eBook Subscription Services
  - Microelectronic Test Structures For Cmos Technology Budget-Friendly Options
6. Navigating Microelectronic Test Structures For Cmos Technology eBook Formats

- ePub, PDF, MOBI, and More
  - Microelectronic Test Structures For Cmos Technology Compatibility with Devices
  - Microelectronic Test Structures For Cmos Technology Enhanced eBook Features
7. Enhancing Your Reading Experience
    - Adjustable Fonts and Text Sizes of Microelectronic Test Structures For Cmos Technology
    - Highlighting and Note-Taking Microelectronic Test Structures For Cmos Technology
    - Interactive Elements Microelectronic Test Structures For Cmos Technology
  8. Staying Engaged with Microelectronic Test Structures For Cmos Technology
    - Joining Online Reading Communities
    - Participating in Virtual Book Clubs
    - Following Authors and Publishers Microelectronic Test Structures For Cmos Technology
  9. Balancing eBooks and Physical Books Microelectronic Test Structures For Cmos Technology
    - Benefits of a Digital Library
    - Creating a Diverse Reading Collection Microelectronic Test Structures For Cmos Technology
  10. Overcoming Reading Challenges
    - Dealing with Digital Eye Strain
    - Minimizing Distractions
    - Managing Screen Time
  11. Cultivating a Reading Routine Microelectronic Test Structures For Cmos Technology
    - Setting Reading Goals Microelectronic Test Structures For Cmos Technology
    - Carving Out Dedicated Reading Time
  12. Sourcing Reliable Information of Microelectronic Test Structures For Cmos Technology
    - Fact-Checking eBook Content of Microelectronic Test Structures For Cmos Technology
    - Distinguishing Credible Sources
  13. Promoting Lifelong Learning
    - Utilizing eBooks for Skill Development
    - Exploring Educational eBooks
  14. Embracing eBook Trends
    - Integration of Multimedia Elements
    - Interactive and Gamified eBooks



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