Formal Verification of Superscalar Microprocessors with Multicycle Functional Units, Exceptions, and Branch Prediction[1]

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Abstract

We extend the Burch and Dill flushing technique [6] for formal verification of microprocessors to be applicable to designs where the functional units and memories have multicycle and possibly arbitrary latency. We also show ways to incorporate exceptions and branch prediction by exploiting the properties of the logic of Positive Equality with Uninterpreted Functions [4][5]. We study the modeling of the above features in different versions of dual-issue superscalar processors.

1 Introduction

In order for formal methods to scale for verification of modern microprocessors, they need to be applicable easily and with a high degree of automation to designs with multicycle functional units, multicycle memories, exceptions, and branch prediction. Burch and Dill's verification methodology has the potential to be highly automatic, but has previously been applied only to designs with single-cycle functional units and memories that produce their results instantaneously [5][6][7][21]. The approach is very elegant in using flushing of the processor—feeding it with bubbles until all instructions in flight complete their execution—in order to compute an abstraction function mapping Implementation states to a Specification state. (The difference between a bubble and a nop is that a bubble does not modify any user-visible state, while a nop increments the PC.) The correctness criterion is a commutative diagram, stating that an application of the transition function of the Implementation followed by flushing should produce the same user-visible state as first flushing the Implementation and then using the resultant user-visible state to apply the transition function of the Specification between 0 and k times, where k is the issue-width of the Implementation. As observed and exploited by Burch in his controlled flushing [7], we can change the logic during flushing, since the only purpose of that logic is to compute an abstraction function. Having an improper abstraction function will not compromise the verification and can only result in a false negative.

The same correctness criterion has been adopted by the theorem-proving community and applied to an out-of-order design with exceptions and interrupts by Sawada and Hunt [17] and to an out-of-order design with only arithmetic instructions by

Hosabettu, Srivas and Gopalakrishnan [13]. However, the former approach requires the user to manually build an intermediate abstraction of the processor and to define a large number of lemmas (Sawada defined nearly 4,000), necessary for the correctness proof. The latter approach requires the user to manually define a set of completion functions, one per unfinished instruction in flight, describing how that instruction will be completed, given that all the instructions that it has data dependencies on have already been completed. Furthermore, the user has to manually define a way to compose these completion functions in order to form the abstraction function for the processor. Both of these theorem-proving methods require months of manual work for complex designs, i.e., they are not automatic.

Not only has the Burch and Dill flushing technique not been applied to processors with multicycle functional units, but Hosabettu, Srivas and Gopalakrishnan [12] have claimed that it has the drawback of being hard to use for pipelines with indeterminate latency, particularly where an ALU computation might have a data-dependent duration or a memory hierarchy of multiple levels might have a non-deterministic delay.

In this work we extend Burch and Dill's flushing-based methodology to be applicable to microprocessors with functional units and memories of multicycle and possibly arbitrary latency. We also model exceptions and branch prediction. Our most complex designs have 10 abstract instruction types. They have two completely functional pipelines, each consisting of five stages, for a total of up to 10 instructions in flight. Therefore, exhaustive binary simulation must consider 10^{10} instruction sequences of 10 instructions each. Furthermore, accounting for possible data dependencies, raised exceptions, correctness/incorrectness of the branch predictions, and multicycle computations will make that number significantly higher. Even directed simulation will probably find it very hard, if at all possible, to generate all interesting instruction sequences for such a design. However, we were able to formally verify it in less than 44 minutes of CPU time.

2 Background

The key to our success is a very efficient decision procedure [21] for the logic of Equality with Uninterpreted Functions and Memories (EUFM) [6], which exploits the properties of Positive Equality [4][5] and the e_{ij} encoding [10] to generate a propositional formula, which is then evaluated with BDDs [3] or SAT-checkers. We found BDDs to be unmatched by SAT-checkers and SVC [18] (a decision procedure for the logic of EUFM that does not exploit Positive Equality) when verifying correct designs. However, SAT-checkers outperform BDDs on buggy processors.

The syntax of EUFM [6] includes terms and formulas. A term can be an Uninterpreted Function (UF) applied on a list of argument terms, a domain variable, or an ITE operator selecting between two argument terms based on a controlling formula, such that $ITE(formula, term1, term2)$ will evaluate to $term1$ when $formula = \textbf{true}$ and to $term2$ when $formula = \textbf{false}$. A formula can be an Uninterpreted Predicate (UP) applied on a list of argu-

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Formal Verification of Microprocessors Miroslav Velev,2015-02-04 Formal verification is the mathematical proof of correctness of computer systems Microprocessors are the most important components in computer systems and are increasingly being used in safety critical applications e g to monitor the health of patients to control the engines and breaks of cars to drive autonomous vehicles and fly autonomous aircraft and to control weapons systems As such the correctness of microprocessors is a matter of public safety and national security Furthermore for the companies that design and manufacture microprocessors or systems controlled by them the correctness of microprocessors is a matter of business success or failure Statistics from industrial microprocessor designs indicate that up to 90% of the engineering effort is spent on verification which increasingly becomes the bottleneck in developing new products Formal verification has the potential to significantly reduce the design time while also guaranteeing complete correctness However previous approaches for formal verification of microprocessors either do not scale for complex designs or require prohibitive amounts of manual effort by experts In contrast this book presents a highly automatic and scalable method for formal verification of complex processors including pipelined superscalar and VLIW designs   **Memory, Microprocessor, and ASIC** Wai-Kai Chen,2003-03-26 Timing memory power dissipation testing and testability are all crucial elements of VLSI circuit design In this volume culled from the popular VLSI Handbook experts from around the world provide in depth discussions on these and related topics Stacked gate embedded and flash memory all receive detailed treatment including their power cons

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Computer-Aided Reasoning Matt Kaufmann,Panagiotis Manolios,J Strother Moore,2013-04-17 Computer Aided Reasoning ACL2 Case Studies illustrates how the computer aided reasoning system ACL2 can be used in productive and innovative ways to design build and maintain hardware and software systems Included here are technical papers written by twenty one contributors that report on self contained case studies some of which are sanitized industrial projects The papers deal with a wide variety of ideas including floating point arithmetic microprocessor simulation model checking symbolic trajectory evaluation compilation proof checking real analysis and several others Computer Aided Reasoning ACL2 Case Studies is meant for two audiences those looking for innovative ways to design build and maintain hardware and software systems faster and more reliably and those wishing to learn how to do this The former audience includes project managers and students in survey oriented courses The latter audience includes students and professionals pursuing rigorous approaches to hardware and software engineering or formal methods Computer Aided Reasoning ACL2 Case Studies can be used in graduate and upper division undergraduate courses on Software Engineering Formal Methods Hardware Design Theory of

Computation Artificial Intelligence and Automated Reasoning The book is divided into two parts Part I begins with a discussion of the effort involved in using ACL2 It also contains a brief introduction to the ACL2 logic and its mechanization which is intended to give the reader sufficient background to read the case studies A more thorough textbook introduction to ACL2 may be found in the companion book Computer Aided Reasoning An Approach The heart of the book is Part II where the case studies are presented The case studies contain exercises whose solutions are on the Web In addition the complete ACL2 scripts necessary to formalize the models and prove all the properties discussed are on the Web For example when we say that one of the case studies formalizes a floating point multiplier and proves it correct we mean that not only can you read an English description of the model and how it was proved correct but you can obtain the entire formal content of the project and replay the proofs if you wish with your copy of ACL2 ACL2 may be obtained from its home page The results reported in each case study as ACL2 input scripts as well as exercise solutions for both books are available from this page

Design of Systems on a Chip: Design and Test Ricardo Reis,Marcelo Soares Lubaszewski,Jochen A.G. Jess,2007-05-06 This book is the second of two volumes addressing the design challenges associated with new generations of semiconductor technology The various chapters are compiled from tutorials presented at workshops in recent years by prominent authors from all over the world Technology productivity and quality are the main aspects under consideration to establish the major requirements for the design and test of upcoming systems on a chip   Proceedings of the ASP-DAC ... Asia and South Pacific Design Automation Conference ,1995   **Formal Verification of Superscalar Microprocessors with Multicycle Functional Units, Exceptions, and Branch Prediction** Miroslav N. Velev,Randal Bryant,2000 Abstract We extend the Burch and Dill flushing technique 6 for formal verification of microprocessors to be applicable to designs where the functional units and memories have multicycle and possibly arbitrary latency We also show ways to incorporate exceptions and branch prediction by exploiting the properties of the logic of Positive Equality with Uninterpreted Functions 4 5 We study the modeling of the above features in different versions of dual issue superscalar processors   **Microprocessor 4** Philippe Darche,2021-02-17 Since its commercialization in 1971 the microprocessor a modern and integrated form of the central processing unit has continuously broken records in terms of its integrated functions computing power low costs and energy saving status Today it is present in almost all electronic devices Sound knowledge of its internal mechanisms and programming is essential for electronics and computer engineers to understand and master computer operations and advanced programming concepts This book in five volumes focuses more particularly on the first two generations of microprocessors those that handle 4 and 8 bit integers Microprocessor 4 the fourth of five volumes addresses the software aspects of this component Coding of an instruction addressing modes and the main features of the Instruction Set Architecture ISA of a generic component are presented Futhermore two approaches are discussed for altering the flow of execution using mechanisms of subprogram and interrupt A comprehensive approach is used with examples drawn from

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