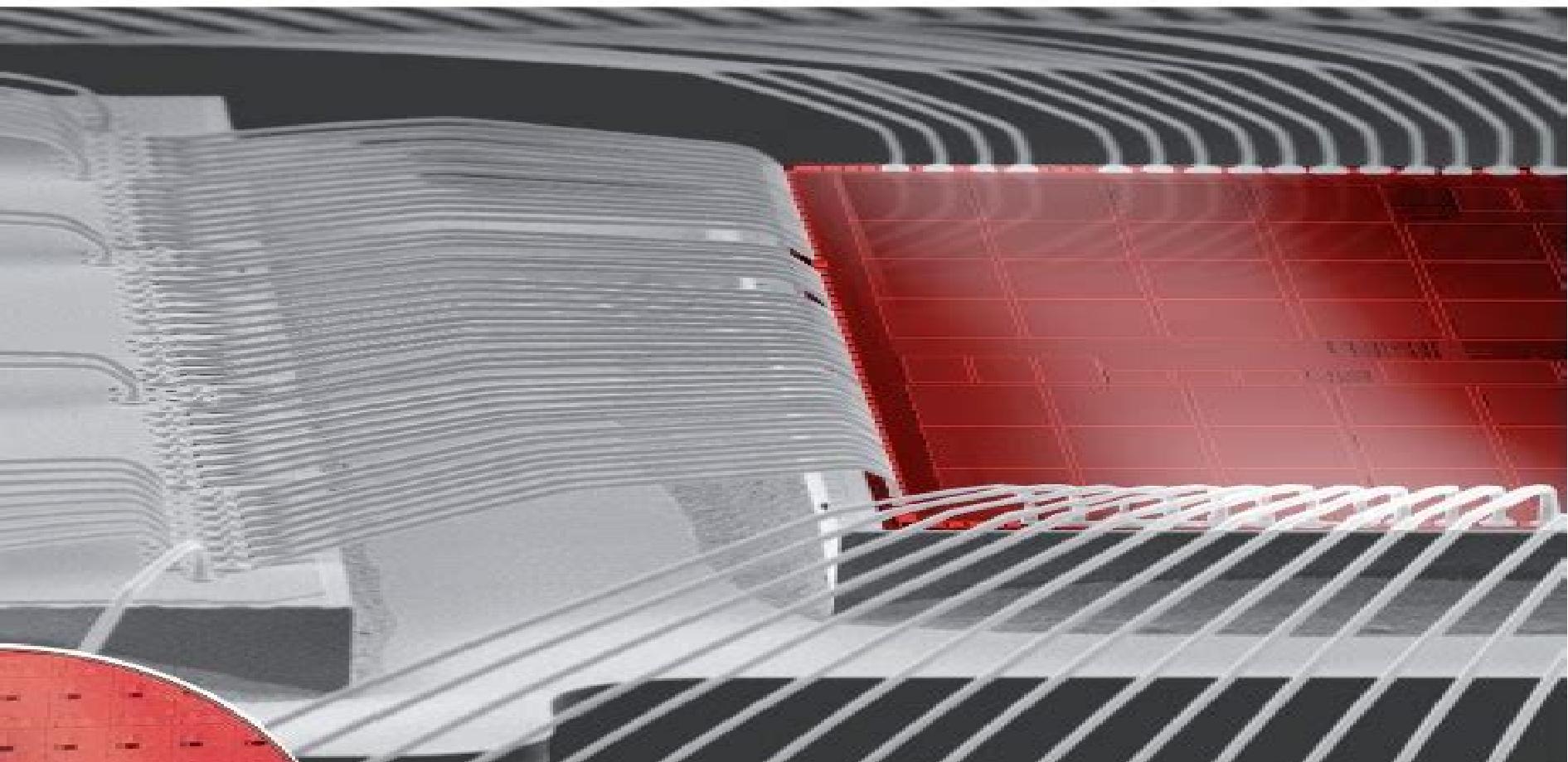


# NANOMETER CMOS ICS

2017 EDITION



From **Basics** to **ASICs**

**Harry Veendrick**

# Nanometer Cmos Nanometer Cmos

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Sansen**

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**Nanometer CMOS RFICs for Mobile TV Applications** Ahmed A. Youssef, James Haslett, 2010-06-17 Nanometer CMOS RFICs for Mobile TV Applications focuses on how to break the trade off between power consumption and performance linearity and noise figure by optimizing the mobile TV front end dynamic range in three hierarchical levels: the intrinsic MOSFET level, the circuit level and the architectural level. It begins by discussing the fundamental concepts of MOSFET dynamic range including nonlinearity and noise. It then moves to the circuit level introducing the challenges associated with designing wide dynamic range variable gain broadband low noise amplifiers.

LNA The book gives a detailed analysis of a new noise canceling technique that helps CMOS LNAs achieve a sub 2 dB wideband noise figure Lastly the book deals with the front end dynamic range optimization process from the systems perspective by introducing the active and passive automatic gain control AGC mechanism [Analog IC Reliability in Nanometer CMOS](#) Elie Maricau,Georges Gielen,2013-01-11 This book focuses on modeling simulation and analysis of analog circuit aging First all important nanometer CMOS physical effects resulting in circuit unreliability are reviewed Then transistor aging compact models for circuit simulation are discussed and several methods for efficient circuit reliability simulation are explained and compared Ultimately the impact of transistor aging on analog circuits is studied Aging resilient and aging immune circuits are identified and the impact of technology scaling is discussed The models and simulation techniques described in the book are intended as an aid for device engineers circuit designers and the EDA community to understand and to mitigate the impact of aging effects on nanometer CMOS ICs [Optoelectronic Circuits in Nanometer CMOS Technology](#) Mohamed Atef,Horst Zimmermann,2016-03-04 This book describes the newest implementations of integrated photodiodes fabricated in nanometer standard CMOS technologies It also includes the required fundamentals the state of the art and the design of high performance laser drivers transimpedance amplifiers equalizers and limiting amplifiers fabricated in nanometer CMOS technologies This book shows the newest results for the performance of integrated optical receivers laser drivers modulator drivers and optical sensors in nanometer standard CMOS technologies Nanometer CMOS technologies rapidly advanced enabling the implementation of integrated optical receivers for high data rates of several Giga bits per second and of high pixel count optical imagers and sensors In particular low cost silicon CMOS optoelectronic integrated circuits became very attractive because they can be extensively applied to short distance optical communications such as local area network chip to chip and board to board interconnects as well as to imaging and medical sensors

*Comparators in Nanometer CMOS Technology* Bernhard Goll,Horst Zimmermann,2014-09-15 This book covers the complete spectrum of the fundamentals of clocked regenerative comparators their state of the art advanced CMOS technologies innovative comparators inclusive circuit aspects their characterization and properties Starting from the basics of comparators and the transistor characteristics in nanometer CMOS seven high performance comparators developed by the authors in 120nm and 65nm CMOS are described extensively Methods and measurement circuits for the characterization of advanced comparators are introduced A synthesis of the largely differing aspects of demands on modern comparators and the properties of devices being available in nanometer CMOS which are posed by the so called nanometer hell of physics is accomplished The book summarizes the state of the art in integrated comparators Advanced measurement circuits for characterization will be introduced as well as the method of characterization by bit error analysis usually being used for characterization of optical receivers The book is compact and the graphical quality of the illustrations is outstanding This book is written for engineers and researchers in industry as well as scientists and Ph D students at universities It is also

recommendable to graduate students specializing on nanoelectronics and microelectronics or circuit design     [Leakage in Nanometer CMOS Technologies](#) Siva G. Narendra,Anantha P. Chandrakasan,2006-03-10 Covers in detail promising solutions at the device circuit and architecture levels of abstraction after first explaining the sensitivity of the various MOS leakage sources to these conditions from the first principles Also treated are the resulting effects so the reader understands the effectiveness of leakage power reduction solutions under these different conditions Case studies supply real world examples that reap the benefits of leakage power reduction solutions as the book highlights different device design choices that exist to mitigate increases in the leakage components as technology scales     [Flip-Flop Design in Nanometer CMOS](#) Massimo

Alioto,Elio Consoli,Gaetano Palumbo,2014-10-14 This book provides a unified treatment of Flip Flop design and selection in nanometer CMOS VLSI systems The design aspects related to the energy delay tradeoff in Flip Flops are discussed including their energy optimal selection according to the targeted application and the detailed circuit design in nanometer CMOS VLSI systems Design strategies are derived in a coherent framework that includes explicitly nanometer effects including leakage layout parasitics and process voltage temperature variations as main advances over the existing body of work in the field The related design tradeoffs are explored in a wide range of applications and the related energy performance targets A wide range of existing and recently proposed Flip Flop topologies are discussed Theoretical foundations are provided to set the stage for the derivation of design guidelines and emphasis is given on practical aspects and consequences of the presented results Analytical models and derivations are introduced when needed to gain an insight into the inter dependence of design parameters under practical constraints This book serves as a valuable reference for practicing engineers working in the VLSI design area and as text book for senior undergraduate graduate and postgraduate students already familiar with digital circuits and timing     [Nanometer CMOS](#) Frank Schwierz,Hei Wong,Juin J. Liou,2010-02-28 This book presents the material necessary for understanding the physics operation design and performance of modern MOSFETs with nanometer dimensions Other topics covered include high k dielectrics and mobility enhancement techniques MOSFETs for RF radio frequency applications MOSFET fabrication technology     [Technische Mechanik](#) Dietmar Gross,Werner Hauger,Walter Schnell,1989

[Leakage in Nanometer CMOS Technologies](#) Siva G. Narendra,Anantha P. Chandrakasan,2005-11-17 Covers in detail promising solutions at the device circuit and architecture levels of abstraction after first explaining the sensitivity of the various MOS leakage sources to these conditions from the first principles Also treated are the resulting effects so the reader understands the effectiveness of leakage power reduction solutions under these different conditions Case studies supply real world examples that reap the benefits of leakage power reduction solutions as the book highlights different device design choices that exist to mitigate increases in the leakage components as technology scales     [Low-Power High-Speed ADCs for Nanometer CMOS Integration](#) Zhiheng Cao,Shouli Yan,2008-07-15 Low Power High Speed ADCs for Nanometer CMOS Integration is about the design and implementation of ADC in nanometer CMOS processes that achieve lower power

consumption for a given speed and resolution than previous designs through architectural and circuit innovations that take advantage of unique features of nanometer CMOS processes A phase lock loop PLL clock multiplier has also been designed using new circuit techniques and successfully tested 1 A 1 2V 52mW 210MS s 10 bit two step ADC in 130nm CMOS occupying 0.38mm<sup>2</sup> Using offset canceling comparators and capacitor networks implemented with small value interconnect capacitors to replace resistor ladder multiplexer in conventional sub ranging ADCs it achieves 74dB SFDR for 10MHz and 71dB SFDR for 100MHz input 2 A 32mW 1 25GS s 6 bit ADC with 2.5GHz internal clock in 130nm CMOS A new type of architecture that combines flash and SAR enables the lowest power consumption 6 bit 1GS s ADC reported to date This design can be a drop in replacement for existing flash ADCs since it does require any post processing or calibration step and has the same latency as flash 3 A 0.4ps rms jitter integrated from 3kHz to 300MHz offset for 2.5GHz 1.3GHz tunable phase noise programmable clock multiplier PLL for generating sampling clock to the SAR ADC A new loop filter structure enables phase error preamplification to lower PLL in band noise without increasing loop filter capacitor size

### **Nanometer CMOS**

**Sigma-Delta Modulators for Software Defined Radio** Alonso Morgado,Rocío del Río,José M. de la Rosa,2011-09-15 This book presents innovative solutions for the implementation of Sigma Delta Modulation SDM based Analog to Digital Conversion ADC required for the next generation of wireless hand held terminals These devices will be based on the so called multi standard transceiver chipsets integrated in nanometer CMOS technologies One of the most challenging and critical parts in such transceivers is the analog digital interface because of the assorted signal bandwidths and dynamic ranges that can be required to handle the A D conversion for several operation modes This book describes new adaptive and reconfigurable SDM ADC topologies circuit strategies and synthesis methods specially suited for multi standard wireless telecom systems and future Software defined radios SDRs integrated in nanoscale CMOS It is a practical book going from basic concepts to the frontiers of SDM architectures and circuit implementations which are explained in a didactical and systematic way It gives a comprehensive overview of the state of the art performance challenges and practical solutions providing the necessary insight to implement successful design through an efficient design and synthesis methodology Readers will learn a number of practical skills from system level design to experimental measurements and testing

**Analog Filters in Nanometer CMOS** Heimo Uhrmann,Robert Kolm,Horst Zimmermann,2013-08-15 Starting from the basics of analog filters and the poor transistor characteristics in nanometer CMOS 10 high performance analog filters developed by the authors in 120 nm and 65 nm CMOS are described extensively Among them are gm C filters current mode filters and active filters for system on chip realization for Bluetooth WCDMA UWB DVB H and LTE applications For the active filters several operational amplifier designs are described The book furthermore contains a review of the newest state of research on low voltage low power analog filters To cover the topic of the book comprehensively linearization issues and measurement methods for the characterization of advanced analog filters are introduced in addition Numerous elaborate

illustrations promote an easy comprehension This book will be of value to engineers and researchers in industry as well as scientists and Ph D students at universities The book is also recommendable to graduate students specializing on nanoelectronics microelectronics or circuit engineering

### **Nanometer CMOS SIGMA-Delta Modulators for Software**

**Defined Radio** ,2011-09-11    **Low-Power High-Level Synthesis for Nanoscale CMOS Circuits** Saraju P.

Mohanty,Nagarajan Ranganathan,Elias Kougianos,Priyadarshan Patra,2008-05-31 Low Power High Level Synthesis for Nanoscale CMOS Circuits addresses the need for analysis characterization estimation and optimization of the various forms of power dissipation in the presence of process variations of nano CMOS technologies The authors show very large scale integration VLSI researchers and engineers how to minimize the different types of power consumption of digital circuits The material deals primarily with high level architectural or behavioral energy dissipation because the behavioral level is not as highly abstracted as the system level nor is it as complex as the gate transistor level At the behavioral level there is a balanced degree of freedom to explore power reduction mechanisms the power reduction opportunities are greater and it can cost effectively help in investigating lower power design alternatives prior to actual circuit layout or silicon implementation The book is a self contained low power high level synthesis text for Nanoscale VLSI design engineers and researchers Each chapter has simple relevant examples for a better grasp of the principles presented Several algorithms are given to provide a better understanding of the underlying concepts The initial chapters deal with the basics of high level synthesis power dissipation mechanisms and power estimation In subsequent parts of the text a detailed discussion of methodologies for the reduction of different types of power is presented including Power Reduction Fundamentals Energy or Average Power Reduction Peak Power Reduction Transient Power Reduction Leakage Power Reduction Low Power High Level Synthesis for Nanoscale CMOS Circuits provides a valuable resource for the design of low power CMOS circuits

**Parametric Analog Signal Amplification Applied to Nanoscale CMOS Technologies** Joao Oliveira,João Goes,2012-01-06 This book is dedicated to the analysis of parametric amplification with special emphasis on the MOS discrete time implementation This implementation is demonstrated by the presentation of several circuits where the MOS parametric amplifier cell is used small gain amplifier comparator with embedded pre amplification discrete time mixer IIR Filter and analog to digital converter ADC Experimental results are shown to validate the overall design technique

**Low-Power Low-Voltage Sigma-Delta Modulators in Nanometer CMOS** Libin Yao,Michiel Steyaert,Willy M Sansen,2006-07-09 Low Power Low Voltage Sigma Delta Modulators in Nanometer CMOS addresses the low power low voltage Sigma Delta ADC design in nanometer CMOS technologies at both the circuit level and the system level The low power low voltage Sigma Delta modulator design at the circuit level is introduced A design example is presented in this book This design is the first published Sigma Delta design in a 90 nm CMOS technology and reaches a very high figure of merit At the system level a novel systematic study on the full feedforward Sigma Delta topology is presented in this book As a design

example a fourth order single loop full feedforward Sigma Delta modulator design in a 130 nm pure digital CMOS technology is presented This design is the first design using the full feedforward Sigma Delta topology and reaches the highest conversion speed among all the 1 V Sigma Delta modulators to date Design of Variation-tolerant Circuits for Nanometer CMOS Technology Mohamed Hassan Abu-Rahma, 2008 Aggressive scaling of CMOS technology in sub 90nm nodes has created huge challenges Variations due to fundamental physical limits such as random dopants fluctuation RDF and line edge roughness LER are increasing significantly with technology scaling In addition manufacturing tolerances in process technology are not scaling at the same pace as transistor s channel length due to process control limitations e g sub wavelength lithography Therefore within die process variations worsen with successive technology generations These variations have a strong impact on the maximum clock frequency and leakage power for any digital circuit and can also result in functional yield losses in variation sensitive digital circuits such as SRAM Moreover in nanometer technologies digital circuits show an increased sensitivity to process variations due to low voltage operation requirements which are aggravated by the strong demand for lower power consumption and cost while achieving higher performance and density It is therefore not surprising that the International Technology Roadmap for Semiconductors ITRS lists variability as one of the most challenging obstacles for IC design in nanometer regime To facilitate variation tolerant design we study the impact of random variations on the delay variability of a logic gate and derive simple and scalable statistical models to evaluate delay variations in the presence of within die variations This work provides new design insight and highlights the importance of accounting for the effect of input slew on delay variations especially at lower supply voltages

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