Embedded Systems

Benny Akesson
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Memory Controllers for Real-Time Embedded Systems

Predictable and Composable Real-Time Systems

Springer

Memory Controllers For Real Time Embedded Systems Predictable And Composable Real Time Systems

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Memory Controllers For Real Time Embedded Systems Predictable And Composable Real Time Systems:

Memory Controllers for Real-Time Embedded Systems Benny Akesson,Kees Goossens,2011-09-15 Verification of real time requirements in systems on chip becomes more complex as more applications are integrated Predictable and composable systems can manage the increasing complexity using formal verification and simulation This book explains the concepts of predictability and composability and shows how to apply them to the design and analysis of a memory controller which is a key component in any real time system *Memory Controllers for Mixed-Time-Criticality Systems* Sven Goossens,Karthik Chandrasekar,Benny Akesson,Kees Goossens,2016-04-11 This book discusses the design and performance analysis of SDRAM controllers that cater to both real time and best effort applications i e mixed time criticality memory controllers The authors describe the state of the art and then focus on an architecture template for reconfigurable memory controllers that addresses effectively the quickly evolving set of SDRAM standards in terms of worst case timing and power analysis as well as implementation A prototype implementation of the controller in SystemC and synthesizable VHDL for an FPGA development board are used as a proof of concept of the architecture template Heterogeneous SoC Design and Verification Khaled Salah Mohamed,2024-03-22 This book covers the foundations of hardware software codesign on chip communication debugging and verification for heterogenous SoCs Its primary objective is to empower designers in making informed decisions guiding them to strike the perfect balance between flexibility and performance for their SoC designs Readers will benefit from a detailed exploration of the essential elements of the hardware and software codesign framework accompanied by a discussion of the driving motivations behind this approach The author also provides an in depth review of various hardware design architectures shedding light on different design possibilities Furthermore the book presents key concepts concerning hardware and software communication unraveling the intricate interactions within an SoC This book provides a holistic introduction to the methodologies underpinning SoC design and verification making it an indispensable companion for both novice and experienced designers navigating the ever evolving landscape of hardware software codesign

Multiprocessor System-on-Chip Michael Hübner,Jürgen Becker,2010-11-25 The purpose of this book is to evaluate strategies for future system design in multiprocessor system on chip MPSoC architectures Both hardware design and integration of new development tools will be discussed Novel trends in MPSoC design combined with reconfigurable architectures are a main topic of concern The main emphasis is on architectures design flow tool development applications and system design *Programming Heterogeneous MPSoCs* Jerónimo Castrillón Mazo,Rainer Leupers,2013-09-24 This book provides embedded software developers with techniques for programming heterogeneous Multi Processor Systems on Chip MPSoCs capable of executing multiple applications simultaneously It describes a set of algorithms and methodologies to narrow the software productivity gap as well as an in depth description of the underlying problems and challenges of today s programming practices The authors present four different tool flows A parallelism extraction flow for applications written

using the C programming language a mapping and scheduling flow for parallel applications a special mapping flow for baseband applications in the context of Software Defined Radio SDR and a final flow for analyzing multiple applications at design time The tool flows are evaluated on Virtual Platforms VPs which mimic different characteristics of state of the art heterogeneous MPSoCs *Annual Index/abstracts of Sae Technical Papers, 2000* Society Of Automotive Engineers,2001 *Computer & Control Abstracts* ,1996 Worst Case Analysis of DRAM Latency in Hard Real Time Systems Zheng Pei Wu,University of Waterloo. Department of Computer Science,2013 As multi core systems are becoming more popular in real time embedded systems strict timing requirements for accessing shared resources must be met In particular a detailed latency analysis for Double Data Rate Dynamic RAM DDR DRAM is highly desirable Several researchers have proposed predictable memory controllers to provide guaranteed memory access latency However the performance of such controllers sharply decreases as DDR devices become faster and the width of memory buses is increased Therefore a novel and composable approach is proposed that provides improved latency bounds compared to existing works by explicitly modeling the DRAM state In particular this new approach scales better with increasing number of cores and memory speed Benchmark evaluation results show up to a 45% improvement in the worst case task execution time compared to a competing predictable memory controller for a system with 16 cores *Dissertation Abstracts International* ,2005 **Scratchpad Memory Management for Multicore Real-time Embedded Systems** Saud Wasly,2018 Multicore systems will continue to spread in the domain of real time embedded systems due to the increasing need for high performance applications This research discusses some of the challenges associated with employing multicore systems for safety critical real time applications Mainly this work is concerned with providing 1 efficient inter core timing isolation for independent tasks and 2 predictable task communication for communicating tasks Principally we introduce a new task execution model based on the 3 phase execution model that exploits the Direct Memory Access DMA controllers available in modern embedded platforms along with ScratchPad Memories SPMs to enforce strong timing isolation between tasks The DMA and the SPMs are explicitly managed to pre load tasks from main memory into the local private scratchpad memories Tasks are then executed from the local SPMs without accessing main memory This model allows CPU execution to be overlapped with DMA loading unloading operations from and to main memory We show that by co scheduling task execution on CPUs and using DMA to access memory and I O we can efficiently hide access latency to physical resources In turn this leads to significant improvements in system schedulability compared to both the case of unregulated contention for access to physical resources and to previous cache and SPM management techniques for real time systems The presented SPM centric scheduling algorithms and analyses cover single core partitioned and global real time systems The proposed scheme is also extended to support large tasks that do not fit entirely into the local SPM Moreover the schedulability analysis considers the case of recovering from transient soft errors bit flips caused by a single event upset in several levels of memories that cannot be automatically

corrected in hardware by the ECC unit The proposed SPM centric scheduling is integrated at the OS level thus it is transparent to applications The proposed scheme is implemented and evaluated on an FPGA platform and a Commercial Off The Shelf COTS platform In regards to real time task communication two types of communication are considered 1 Asynchronous inter task communication between either sequential tasks single threaded or parallel tasks multi threaded 2 Intra task communication where parallel threads of the same application exchange data A new task scheduling model for parallel tasks Bundled Scheduling is proposed to facilitate intra task communication and reduce synchronization overheads We show that the proposed bundled scheduling model can be applied to several parallel programming models such as fork join and DAG based applications leading to improved system schedulability Finally intra task communication is governed by a predictable inter core communication platform Specifically we propose HopliteRT a lean and predictable Network on Chip that connects the private SPMs Predictable and Monitored Execution for COTS-based Real-time Embedded Systems Rodolfo Pellizzoni,2010 Modern real time embedded systems are moving from federated architectures where logical applications and subsystems are implemented on different hardware components to progressively more integrated architectures which use extensive sharing of different physical resources These systems employ multiple active components such as CPU cores HW processors coprocessors and peripherals which can all autonomously perform computational and communication activities Furthermore they are increasingly built using Commercial Off The Shelf COTS components in an attempt to increase performance and reduce cost and time to market Integrated real time systems such as those employed in the avionic medical and automotive domain are often mixed criticality systems they implement different applications with widely varying levels of criticality Therefore a key issue is to provide sufficient isolation among different applications In particular safety critical applications can expose requirements both in terms of functional isolation e g fault containment and in terms of physical isolation e g safe sharing of physical resources such as CPU and communication time memory and power In this work we study the design of mechanisms and policies to support both functional and physical isolation with a special focus on timing guarantees In particular since most available COTS components do not provide sufficient hardware isolation mechanisms we propose the concept of a control abstraction an unintrusive hardware device or software layer that is interposed between a COTS component and the rest of the system allowing the system architect to predictably control all its resource accesses By employing control abstractions unverified COTS components can be used to implement low criticality but high performance applications while still providing all required isolation guarantees to safety critical modules Functional isolation is provided by monitoring the run time communication behavior of the component against a formal specification and taking a recovery action whenever the specification is violated Timing isolation is provided by coscheduling all computational and communication activities in such as way that there is no contention for access to system resources We show the validity of our methodology by applying it to two different embedded architectures For System on Chip architectures we detail a

complete platform based design process that automatically generates control abstractions for all integrated processors from a high level functional system specification We test the described design process on the case study of a medical pacemaker For COTS based computational nodes we focus on the contention between CPU tasks and peripherals for access both to shared communication infrastructures such as PCI and to main memory Our experiments show that main memory interference can greatly increase the worst case execution time of a task up to almost 200% for a dual core system with a single PCIe peripheral To overcome this issue we propose both analysis techniques to compute upper bounds on the worst case task delay as well as hardware and software control abstractions to reduce such delay In particular we detail the design and implementation of a new hardware device the real time bridge which is interposed between each COTS peripheral and the PCI bus The real time bridge buffers all incoming outgoing traffic to from the peripheral and delivers it predictably according to a defined schedule Furthermore we propose to execute CPU tasks according to a new PRedictable Execution Model PREM which uses a combination of compiler techniques and OS modifications to precisely control all main memory accesses performed by a task By combining PREM with the real time bridge we can coschedule all accesses in main memory by both peripherals and tasks thus eliminating low level contention and unpredictable access delays Our experiments show reductions in worst case execution time up to 40% 60% compared to a traditional execution model A Dynamic Scratchpad Memory Unit for Predictable Real-time Embedded Systems Saud Wasly,2012 Scratch pad memory is a popular alternative to caches in real time embedded systems due to its advantages in terms of timing predictability and power consumption However dynamic management of scratch pad content is challenging in multitasking environments To address this issue this thesis proposes the design of a novel Real Time Scratchpad Memory Unit RSMU The RSMU can be integrated into existing systems with minimal architectural modi cations Furthermore scratchpad management is performed at the OS level requiring no application changes In conjunction with a two level scheduling scheme the RSMU provides strong timing guarantees to critical tasks Demonstration and evaluation of the system design is provided on an embedded FPGA platform

Predictable Shared Memory Resources for Multi-core Real-time Systems Mohamed Hassan,2017 A major challenge in multi core real time systems is the interference problem on the shared hardware components amongst cores Examples of these shared components include buses on chip caches and off chip dynamic random access memories DRAMs The problem arises because different cores in the system interfere with each other while competing to access the shared hardware components It is a challenging problem for real time systems because operations of one core affect the temporal behaviour of other cores which complicates the timing analysis of the system We address this problem by making the following contributions 1 For shared buses we propose CArb a predictable and criticality aware arbiter which provides guaranteed and differential service to tasks based on their requirements In addition we utilize CArb to mitigate overheads resulting from system switching among different modes 2 For the cache hierarchy we address the problem of maintaining

cache coherence in multi core real time systems by modifying current coherence protocols such that data sharing is viable for real time systems in a manner amenable for timing analysis The proposed solution provides performance improvements does not impose any scheduling restrictions and does not require any source code modifications 3 At the shared DRAM level we propose PMC a programmable memory controller that provides latency guarantees for running tasks upon accessing the off chip DRAM while assigning differential memory services to tasks based on their bandwidth and latency requirements In addition to PMC we conduct a latency based analysis on DRAM memory controllers MCs Our analysis provides both best case and worst case bounds on the latency that any request suffers upon accessing the DRAM The analysis comprehensively covers all possible interactions of successive requests considering all possible DRAM states Finally we formally model request interrelations and DRAM command interactions We use these models to develop an automated validation framework along with benchmark suites to validate and evaluate PMC and any other MC which we release as an open source tool **A Comprehensive Study of DRAM Controllers in Real-time Systems** Danlu Guo,2016 The DRAM main memory is a critical component and a performance bottleneck of almost all computing systems Since the DRAM is a shared memory resource on multi core plat forms all cores contend for the memory bandwidth Therefore there is a keen interest in the real time community to design predictable DRAM controllers to provide a low memory access latency bound to meet the strict timing requirement of real time applications Due to the lack of generalization of publicly available DRAM controller models in full system and DRAM device simulators researchers often design in house simulator to validate their designs An extensible cycle accurate DRAM controller simulation frame work is developed to simplify the process of validating new DRAM controller designs To prove the extensibility and reusability of the framework ten state of the art predictable DRAM controllers are implemented in the framework with less than 200 lines of new code With the help of the framework a comprehensive evaluation of state of the art pre dictable DRAM controllers is performed analytically and experimentally to show the im pact of different system parameters This extensive evaluation allows researchers to assess the contribution of state of the art DRAM controller approaches At last a novel DRAM controller with request reordering technique is proposed to provide a configurable trade off between latency bound and bandwidth in mixed critical systems Compared to the state of the art DRAM controller there is a balance point between the two designs which depends on the locality of the task under analysis and the DRAM device used in the system **Memory Allocation for Real-Time Embedded Systems** Sangyeol Kang,2012

Adaptive Real-Time Embedded Systems Tom Springer,2015 Modern embedded systems are required to work in ever increasing dynamic environments where predicting the computational load on those systems is intractable However timely responses to events have to be provided within precise timing constraints in order to guarantee a required level of performance Consequently embedded systems by their very nature exhibit real time characteristics which impose an additional set of restrictions than those in a typical general purpose system In addition to the limitations of having to perform

to strict timing constraints most embedded systems are constrained by size weight energy consumption and cost limitations As a result efficient resource management is a critical aspect in embedded systems that must be considered at multiple architectural levels The main objective of this work is to present our work on real time systems that progress to make the next generation embedded systems more predictable and adaptive to dynamic computational changes To achieve these goals this phase of our research has focused on the resource synchronization and adaptive scheduling of real time embedded applications in uni processor and multi core environments The analysis and experiments show that our resource synchronization protocols outperformed other state of the art resource access control protocols used in hierarchical scheduled systems Implemented in VxWorks and applied to applications used in the aerospace industry response times for hard real time tasks were improved and deadline misses for hard real time tasks were substantially reduced

Schedulability-driven Scratchpad Memory Swapping for Resource-constrained Real-time Embedded Systems Michael P. De Francis,2012 In resource constrained real time embedded systems scratchpad memory SPM is utilized in place of cache to increase performance and enforce consistent behavior of both hard and soft real time tasks via software controlled SPM management techniques SPMMTs Real time systems depend on time critical hard tasks to complete execution before their deadline time Many real time systems also depend on the execution of soft tasks that do not have to complete by hard deadlines This thesis evaluates a new SPMMT that increases both worst case task slack time TST and soft task processing capabilities by combining two existing SPMMTs The schedulability driven ACETRB WCETRB swapping SDAWS SPMMT of this thesis uses task schedulability characteristics to control the selection of either the average case execution time reduction based ACETRB SPMMT or the worst case execution time reduction based WCETRB SPMMT While the literature contains examples of combined management techniques until now there have been none that combine both WCETRB and ACETRB SPMMTs The advantage of combining them is to achieve WCET reduction comparable to what can be achieved with the WCETRB SPMMT while achieving significantly reduced ACET relative to the WCETRB SPMMT Using a stripped down RTOS and an SPMMT simulator implemented for this work evaluated resource constrained scenarios show a reduction in task slack time from the SDAWS SPMMT relative to the WCETRB SPMMT between 20% and 45% However the evaluated scenarios also conservatively show that SDAWS can reduce ACET relative to the WCETRB SPMMT by up to 60% For the evaluated scenarios the smallest slack time and largest ACET reduction are seen when the SPM swap time SPMST to task WCET ratio is minimized Though a SPMST WCET ratio of 1 5 or greater reduced slack times under SDAWS versus the ACETRB SPMMT a SPMST WCET ratio of 1 100 resulted in slack times up to 200% larger than those under the ACETRB SPMMT Thus for systems that can provide small SPMST WCET ratios SDAWS can provide significant ACET reduction while maintaining the majority of slack time assurance provided under WCETRB SPM management Abstract **Advanced Memory Optimization Techniques for Low-Power Embedded Processors** Manish Verma,Peter Marwedel,2007-06-20 In a relatively short span of

time computers have evolved from huge mainframes to small and elegant desktop computers and now to low power ultra portable handheld devices Witheachpassinggeneration computersconsistingofprocessors memoriesandperipherals becamesmallerandfaster Forexample the rstcommercialcomputerUNIVACIcosted 1 million dollars occupied 943 cubic feet space and could perform 1 905 operations per second 94 Now a processor present in an electric shaver easily outperforms the early mainframe computers The miniaturization is largely due to the efforts of engineers and scientists that made the expeditious progress in the microelectronic technologies possible According to Moore s Law 90 the advances in technology allow us to double the number of transistors on a single silicon chip every 18 months This has lead to an exponential increase in the number of transistors on a chip from 2 300 in an Intel 4004 to 42 millions in Intel Itanium processor 55 Moore s Law has withstood for 40 years and is predicted to remain valid for at least another decade 91 Notonlytheminiaturizationanddramaticperformanceimprovementbutalsothesign icantdropinthepriceofprocessors hasleadtosituationwheretheyarebeingintegratedinto products such as cars televisions and phones which are not usually associated with c puters This new trend has also been called the disappearing computer where the computer does not actually disappear but it is everywhere 85 Digital devices containing processors now constitute a major part of our daily lives Asmalllistofsuchdevicesincludesmicrowaveovens televisionsets mobilephones digital cameras MP3 players and cars Whenever a system comprises of information processingdigitaldevicestocontrolortoaugmentitsfunctionality suchasystemistermedanembedded system Therefore all the above listed devices can be also classi ed as embedded systems

Fast, Efficient and Predictable Memory Accesses Lars Wehmeyer,Peter Marwedel,2006-09-08 Speed improvements in memory systems have not kept pace with the speed improvements of processors leading to embedded systems whose performance is limited by the memory This book presents design techniques for fast energy efficient and timing predictable memory systems that achieve high performance and low energy consumption In addition the use of scratchpad memories significantly improves the timing predictability of the entire system leading to tighter worst case execution time bounds

Providing Predictability for High End Embedded Systems ,2001 Real Time systems require logical and temporal correctness Temporal correctness implies that each task running on the system has a deadline that needs to be met To ensure that the deadlines are met the scheduler of a real time system needs information about the worst case execution time WCET of each task The task of determining the WCET of a task on a particular architecture is called timing analysis Analysis techniques are broadly classified as static and dynamic Dynamic timing analysis does not provide safe WCET bounds Static analysis cannot be used on modern processors with features like out of order execution dynamic branch prediction and speculative execution Such features while improving the average case performance induce counter intuitive timing behavior known as timing anomalies Hence designers of hard real time systems are forced to use architectures with simple in order pipelines This thesis develops and demonstrates the benefits of a hybrid timing analysis technique combining static and

dynamic analysis on a processor simulator and on FPGA hardware to provide tight and safe WCET bounds The technique makes the following contributions It enhances the realm of design for hard real time systems by allowing the designers to use complex out of order architectures that exhibit timing anomalies It eliminates the need for complex prototyping of hardware for static timing analysis since the analysis can be done directly on the actual hardware This has the added advantage of eliminating timing inaccuracies arising out of variations in manufacturing technology The method helps manufacturers to protect their Intellectual Property by eliminating the need to disclose architectural details for the purpose of static timing analysis

Reviewing **Memory Controllers For Real Time Embedded Systems Predictable And Composable Real Time Systems**: Unlocking the Spellbinding Force of Linguistics

In a fast-paced world fueled by information and interconnectivity, the spellbinding force of linguistics has acquired newfound prominence. Its capacity to evoke emotions, stimulate contemplation, and stimulate metamorphosis is actually astonishing. Within the pages of "**Memory Controllers For Real Time Embedded Systems Predictable And Composable Real Time Systems**," an enthralling opus penned by a highly acclaimed wordsmith, readers set about an immersive expedition to unravel the intricate significance of language and its indelible imprint on our lives. Throughout this assessment, we shall delve to the book is central motifs, appraise its distinctive narrative style, and gauge its overarching influence on the minds of its readers.

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