

High speed serial link design (SERDES)

Introduction, Architectures and applications

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Abstract This paper describes basic methods of transferring data through serial data buses, using serializer-deserializer (SerDes) as main device in this operation. It explains function of SerDes and different techniques for implementing it.

Keywords: SERDES, Clock and data recovery, High speed SerDes, Parallel clock SERDES, Embedded clock SERDES, Shared SERDES, Bit interleaving SERDES

I. INTRODUCTION

The simplest method of transferring data through the inputs or outputs of a silicon chip is to directly connect the datapath from one chip to the next chip. Since data often consist of more than one bit of information, the datapath is more than one-bit wide.

There are two inherent problems of the parallel data bus. The first problem is that n input/output (I/O) pins are required on each chip to transfer the data. The second problem involves meeting timing requirements. Due to these two problems we thought about transforming parallel data to serial streams of data to be able to use serial communications off-chips and on-chips.

Serializers/Deserializers (SerDes) are the main devices which convert parallel data into stream of serial data and send it through a channel.

Serial interconnects form the critical backbone of modern communication systems, so the choice of SerDes can have a big impact on system cost and performance. While the range of choices may seem confusing at first, SerDes devices fall into a few basic architectures, each tailored to specific application requirements. A basic understanding of these architectural differences enables the designer to quickly find the right SerDes for the application. In this paper we examine four distinct SerDes architectures and show how each plays a vital role in today's systems.

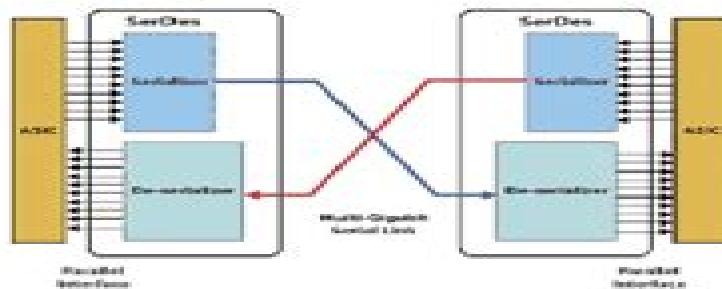


Fig. 1 serial-to-parallel device

II. ARCHITECTURE OF HIGH-SPEED SERDES

High-speed Serializer/Deserializer (HSS) devices are the dominant implementation of I/O interfaces at speed of 2.5 Gbps and higher. Such devices are differentiated from source-synchronous interface in that the receiver device contains a clock data recovery (CDR) circuit dynamically determines the optimal sampling point of the data signal based upon the transition edges of the signal. In other words clock information is extracted directly from the data rather than relying on a separate clock.



Fig. 2 HSS basic block diagram

Fig. 2 illustrate the basic block diagram of the transmit and receive channels of an HSS device. The transmitter serializes parallel data, equalizes it and then drives the serial data onto a differential signal pair of interconnect wires. The receiver consists of a differential receiver, a CDR circuit which may also integrate an equalizer and deserializes the data upon the sample point established by the CDR.

SerDes cores which contain only transmit or only receive channels are called **simplex cores**; SerDes cores which contain both transmit and receive channels are called **full duplex cores**. Note that the terminology "full duplex" does not imply that the electrical interface is bidirectional. Any given electrical interconnect channel has a fixed direction of data transmission. If a protocol application requires "full duplex" communication, then independent transmit and receive channels with independent interconnections are used to implement the interface.



Simplex core, no Rx block



Full Duplex core, Rx and Tx over the same A



Half-Duplex core, Rx and Tx over the same A

Fig. 3 different types of serdes cores

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Efficient Test Methodologies for High-Speed Serial Links Dongwoo Hong,Kwang-Ting Cheng,2009-12-24 Efficient Test Methodologies for High Speed Serial Links describes in detail several new and promising techniques for cost effectively testing high speed interfaces with a high test coverage One primary focus of Efficient Test Methodologies for High Speed Serial Links is on efficient testing methods for jitter and bit error rate BER which are widely used for quantifying the quality of a communication system Various analysis as well as experimental results are presented to demonstrate the validity of the presented techniques

High Speed Serdes Devices and Applications David Robert Stauffer,Jeanne Trinko

Mechler,Michael A. Sorna,Kent Dramstad,Clarence Rosser Ogilvie,Amanullah Mohammad,James Donald

Rockrohr,2008-12-19 The simplest method of transferring data through the inputs or outputs of a silicon chip is to directly connect each bit of the datapath from one chip to the next chip Once upon a time this was an acceptable approach However one aspect and perhaps the only aspect of chip design which has not changed during the career of the authors is Moore's Law which has dictated substantial increases in the number of circuits that can be manufactured on a chip The pin densities of chip packaging technologies have not increased at the same pace as has silicon density and this has led to a prevalence of High Speed Serdes HSS devices as an inherent part of almost any chip design HSS devices are the dominant form of input output for many if not most high integration chips moving serial data between chips at speeds up to 10 Gbps and beyond Chip designers with a background in digital logic design tend to view HSS devices as simply complex digital input output cells This view ignores the complexity associated with serially moving billions of bits of data per second At these data rates the assumptions associated with digital signals break down and analog factors demand consideration The chip designer who oversimplifies the problem does so at his or her own peril

High Speed VCSELs for Optical Interconnects Alex

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Machine Learning-based Design and Optimization of High-Speed Circuits Vazgen Melikyan,2023-12-30 This book describes machine learning based new principles methods of

design and optimization of high speed integrated circuits included in one electronic system which can exchange information between each other up to 128 256 512 Gbps speed The efficiency of methods has been proven and is described on the examples of practical designs This will enable readers to use them in similar electronic system designs The author demonstrates newly developed principles and methods to accelerate communication between ICs working in non standard

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Jitter, Noise, and Signal Integrity at High-Speed Mike Peng Li,2007-11-19 State of the art JNB and SI Problem Solving Theory Analysis Methods and Applications Jitter noise and bit error JNB and signal integrity SI have become today s greatest challenges in high speed digital design Now there s a comprehensive and up to date guide to overcoming these challenges direct from Dr Mike Peng Li cochair of the PCI Express jitter standard committee One of the field s most respected experts Li has brought together the latest theory analysis methods and practical applications demonstrating how to solve difficult JNB and SI problems in both link components and complete systems Li introduces the fundamental terminology definitions and concepts associated with JNB and SI as well as their sources and root causes He guides readers from basic math statistics circuit and system models all the way through final applications Emphasizing clock and serial data communications applications he covers JNB and SI simulation modeling diagnostics debugging compliance testing and much more

System-on-Chip Test Architectures Laung-Terng Wang,Charles E. Stroud,Nur A. Touba,2010-07-28 Modern electronics testing has a legacy of more than 40 years The introduction of new technologies especially nanometer technologies with 90nm or smaller geometry has allowed the semiconductor industry to keep pace with the increased performance capacity demands from consumers As a result semiconductor test costs have been growing steadily and typically amount to 40% of today s overall product cost This book is a comprehensive guide to new VLSI Testing and Design for Testability techniques that will allow students researchers DFT practitioners and VLSI designers to master quickly System on Chip Test architectures for test debug and diagnosis of digital memory and analog mixed signal designs Emphasizes VLSI Test principles and Design for Testability architectures with numerous illustrations examples Most up to date coverage available including Fault Tolerance Low Power Testing Defect and Error Tolerance Network on Chip NOC Testing Software Based Self Testing FPGA Testing MEMS Testing and System In Package SIP Testing which are not yet available in any testing book Covers the entire spectrum of VLSI testing and DFT architectures from digital and analog to memory circuits and fault diagnosis and self repair from digital to memory circuits Discusses future nanotechnology test trends and challenges facing the nanometer design era promising nanotechnology test techniques including Quantum Dots Cellular Automata Carbon Nanotubes and Hybrid Semiconductor Nanowire Molecular Computing Practical problems at the end of each chapter for students

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Journal of Southeast University ,2004 Electronic Design ,2001 Network Congestion Control Michael Welzl,2005-09-02 As the Internet becomes increasingly heterogeneous the issue of congestion control becomes ever more important In order to maintain good network performance mechanisms must be provided to prevent the network from being congested for any significant period of time Michael Welzl describes the background and concepts of Internet congestion control in an accessible and easily comprehensible format Throughout the book not just the how but the why of complex technologies including the Transmission Control Protocol TCP and Active Queue Management are explained The text also gives an overview of the state of the art in congestion control research and an insight into the future Network Congestion Control Presents comprehensive easy to read documentation on the advanced topic of congestion control without heavy maths Aims to give a thorough understanding of the evolution of Internet congestion control how TCP works why it works the way it does and why some congestion control concepts failed for the Internet Explains the Chiu Jain vector diagrams and introduces a new method of using these diagrams for analysis teaching design Elaborates on how the theory of congestion control impacts on the practicalities of service delivery Includes an appendix with examples problems to assist learning Provides an accompanying website with Java tools for teaching congestion control as well as examples links to code and projects bibliography This invaluable text will provide academics and researchers in computer science electrical engineering and communications networking as well as students on advanced networking and Internet courses with a thorough understanding of the current state and future evolution of Internet congestion control Network administrators and Internet service and applications providers will also find Network Congestion Control a comprehensive accessible self teach tool

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