Formal Verification of a Superscalar Execution Unit[1]

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Abstract. Many modern systems are designed as a set of interconnected reactive subsystems. The subsystem verification task is to verify an implementation of the subsystem against the simple deterministic high-level specification of the entire system. Our verification methodology, based on Symbolic Trajectory Evaluation, is able to bridge the wide gap between the abstract specification and the implementation specific details of the subsystem. This paper presents a detailed description of an industrial application of this methodology to the fixed point execution unit of the PowerPC processor. We were able to verify a representative instruction under all possible stall, bypass, pipeline conditions and under all possible timings for interface to other functional units in the processor.

1. Introduction

Some modern systems with a simple deterministic high-level specification have implementations that exhibit highly nondeterministic behaviors. A large class of systems that exhibit such behavior are processors. At the high-level the sequencing model inherent in processors is the sequential execution model. However, at the low level, these processors are implemented as a set of interconnected reactive subsystems. The subsystems have complex interfaces and use nondeterministic protocols to interact with each other. In addition, the underlying implementation of subsystems uses features such as pipelines and dispatching multiple instruction per cycle in an effort to increase performance. The interaction among instructions results in increased interlock and resource conflict problems which leads to nondeterminism in the subsystem. Such subsystems contain many subtle features with the potential for serious design error.

A methodology for formal verification of such subsystems presents a unique set of challenges. The goal is to verify the implementation of the subsystem against the more natural high-level specification of the entire system. The verification methodology has to incorporate the ability of defining the environment around the subsystem. The environment defines the set of restrictions and requirements placed on the subsystem by the rest of the system. The restrictions and requirements are usually in the form of a set of nondeterministic protocols defined on the interface signals. In addition to defining these interfaces, the methodology has to account for complex features such as instruction pipelines, pipeline interlocks, multiple instruction issue, multiple cycle instructions and speculative execution. Though formal verification tools have started gaining acceptance in the industry[8][9][10][11], they do not provide a rigorous methodology for subsystem verification.

Our verification methodology is able to bridge the wide gap between the abstract specification of the entire system and the sub-

systems" often radical deviation from the sequential execution model. This paper focuses on applying our methodology to verify the fixed point unit of a PowerPC processor. The fixed point unit represents a subsystem with a complex interface and several of the performance enhancing features found in modern day processors.

A high level overview of our methodology for subsystem verification and some of the related work is presented in Section 2. Section 3 discusses the implementation details of the fixed point unit. The steps required by our methodology to verify the fixed point unit are detailed in Section 4. The results of the verification are presented in Section 5.

2. Overview of Verification Methodology

The goal is to develop a methodology with which a designer can show that an implementation of the subsystem correctly fulfills an abstract specification of the desired system behavior. The abstract specification describes the high-level behavior of the system independent of any timing or implementation details. As an example, the natural specification of a processor is the instruction set architecture. The specification is a set of *abstract assertions* defining the effect of each operation on user-visible state elements. The verification process must bridge a wide gap between the detailed subsystem implementation and the abstract specification. In spanning this gap, the verifier must account for issues such as system clocking, pipelines and interfaces with other subsystems. To bridge this gap, the verification process requires some additional mapping information. The *implementation mapping* relates the abstract state elements in the assertions to signals in the subsystem. The implementation mapping is a nondeterministic mapping defined in terms of state diagrams. State diagrams allow users to create an environment around the subsystem and define complex nondeterministic interface protocols. The state diagrams corresponding to the inputs can be viewed as generators that generate low-level signals required for the operation of the subsystem. State diagrams corresponding to outputs can be viewed as acceptors that recognize low-level signals on the outputs of the subsystem. In addition to defining the environment, the mapping also has information about how to stitch instructions together to create infinite execution sequences.

The abstract specification and the implementation mapping are used to generate the *trajectory specification*. The trajectory specification consists of a set of *trajectory assertions*. Each abstract assertion gets mapped into a trajectory assertion. The trajectory assertion captures all possible sequences of circuit state that arise due to nondeterministic interactions of the signals in the environment around the subsystem. A modified form of symbolic simulation called Symbolic Trajectory Evaluation (STE)[1] is used to verify the trajectory assertions on the subsystem.

The reader is referred to [4] for a more detailed description of our verification methodology.

2.1. Related Work

Beatty[2] laid down the foundation for our methodology for formal verification of systems. However his work had one basic limitation. The methodology could handle only bounded single behavior sequences. We have extended the methodology to handle a greater level of nondeterministic behavior required for subsystem verifica-

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Integrated Formal Methods Paula Herber,Anton Wijs,2023-11-10 This volume LNCS 14300 constitutes the refereed proceedings of the 18th International Conference IFM 2023 in November 2023 held in Leiden The Netherlands The 16 full papers presented together with 2 short papers were carefully reviewed and selected from 51 submissions The conference focuses on all aspects of the design of integrated techniques including language design verification and validation automated tool support and the use of such techniques in software engineering practice *Formal Methods in Computer-Aided Design* Ganesh Gopalakrishnan,Phillip Windley,2003-07-31 This book constitutes the refereed proceedings of the Second International Conference on Formal Methods in Computer Aided Design FMCAD 98 held in Palo Alto California USA in November 1998 The 27 revised full papers presented were carefully reviewed and selected from a total of 55 submissions Also included are four tools papers and four invited contributions The papers present the state of the art in formal verification methods for digital circuits and systems including processors custom VLSI circuits microcode and reactive software From the methodological point of view binary decision diagrams model checking symbolic reasoning symbolic simulation and abstraction methods are covered **Formal Verification of Microprocessors** Miroslav Velev,2015-02-04 Formal verification is the mathematical proof of correctness of computer systems Microprocessors are the most important components in computer systems and are increasingly being used in safety critical applications e g to monitor the health of patients to control the engines and breaks of cars to drive autonomous vehicles and fly autonomous aircraft and to control weapons systems As such the correctness of microprocessors is a matter of public safety and national security Furthermore for the companies that design and manufacture microprocessors or systems controlled by them the correctness of microprocessors is a matter of business success or failure Statistics from industrial microprocessor designs indicate that up to 90% of the engineering effort is spent on verification which increasingly becomes the bottleneck in developing new products Formal verification has the potential to significantly reduce the design time while also guaranteeing complete correctness However previous approaches for formal verification of microprocessors either do not scale for complex designs or require prohibitive amounts of manual effort by experts In contrast this book presents a highly automatic and scalable method for formal verification of complex processors including pipelined superscalar and VLIW designs Logic for Programming, Artificial Intelligence, and Reasoning Nikolaj Bjørner,Andrei Voronkov,2012-02-24 This book constitutes the proceedings of the 18th International Conference on Logic for Programming Artificial Intelligence and Reasoning LPAR 18 held in Merida Venezuela in March 2012 The 25 regular papers and 6 tool descriptions and experimental papers presented were carefully reviewed and selected from 74 submissions The series of International Conferences on Logic for Programming Artificial Intelligence and Reasoning LPAR is a forum where year after year some of the most renowned researchers in the areas of logic automated reasoning computational logic programming languages and their applications come to present

cutting edge results to discuss advances in these fields and to exchange ideas in a scientifically emerging part of the world

Theory and Applications of Satisfiability Testing Enrico Giunchiglia,2004-01-26 This book constitutes the thoroughly refereed post proceedings of the 6th International Conference on Theory and Applications of Satisfiability Testing SAT 2003 held in Santa Margherita Ligure Italy in May 2003 The 33 revised full papers presented together with 5 articles reporting results of the related SAT competition and QBF evaluation were carefully selected during two rounds of reviewing and improvement from 67 submissions The whole spectrum of research in propositional and quantified Boolean formula satisfiability testing is covered including proof systems search techniques probabilistic analysis of algorithms and their properties problem encodings industrial applications specific tools case studies and empirical results *Microelectronics Education* Adrian M. Ionescu,Michel Declercq,Maher Kayal,Yusuf Leblebici,2013-03-19 In this book key contributions on developments and challenges in research and education on microelectronics microsystems and related areas are published Topics of interest include but are not limited to emerging fields in design and technology new concepts in teaching multimedia in microelectronics industrial roadmaps and microelectronic education curricula nanoelectronics teaching long distance education The book is intended for academic education level and targets professors researchers and PhDs involved in microelectronics and or more generally in electrical engineering microsystems and material sciences The 2004 edition of European Workshop on Microelectronics Education EWME is particularly focused on the interface between microelectronics and bio medical sciences *The Handbook on Reasoning-Based Intelligent Systems* Kazumi Nakamatsu,2013 This book consists of various contributions in conjunction with the keywords OC reasoningOCO and OC intelligent systemsOCO which widely covers theoretical to practical aspects of intelligent systems Therefore it is suitable for researchers or graduate students who want to study intelligent systems generally Principles and Practice of Constraint Programming ,2003

Formal Verification of Superscalar Microprocessors with Multicycle Functional Units, Exceptions, and Branch Prediction Miroslav N. Velev,Randal Bryant,2000 Abstract We extend the Burch and Dill flushing technique 6 for formal verification of microprocessors to be applicable to designs where the functional units and memories have multicycle and possibly arbitrary latency We also show ways to incorporate exceptions and branch prediction by exploiting the properties of the logic of Positive Equality with Uninterpreted Functions 4 5 We study the modeling of the above features in different versions of dual issue superscalar processors *Proceedings of the 36th Annual IEEE/ACM International Symposium on Microarchitecture* ,2003 MICRO 36 discusses new microarchitecture and software techniques and explores the latest research related to processor architecture compilers and systems for technical interaction on traditional MICRO topics The proceedings also places a special emphasis on optimizations that take advantage of application specific opportunities In addition this year s MICRO includes papers that will benefit both the microarchitecture and embedded architecture communities **Proceedings** ,2000 *ISLPED '00* ,2000 *A Systematic Methodology for Verifying Superscalar*

Microprocessors Mandayam Srivas,1999 *Automatic Generation of Invariants in Formal Verification of Microprocessors and Memory Systems* Husam Saad Abu-Haimed,2004 **Design and Verification of Microprocessor Systems for High-Assurance Applications** David S. Hardin,2010-03-02 Microprocessors increasingly control and monitor our most critical systems including automobiles airliners medical systems transportation grids and defense systems The relentless march of semiconductor process technology has given engineers exponentially increasing transistor budgets at constant recurring cost This has encouraged increased functional integration onto a single die as well as increased architectural sophistication of the functional units themselves Additionally design cycle times are decreasing thus putting increased schedule pressure on engineers Not surprisingly this environment has led to a number of uncaught design flaws Traditional simulation based design verification has not kept up with the scale or pace of modern microprocessor system design Formal verification methods offer the promise of improved bug finding capability as well as the ability to establish functional correctness of a detailed design relative to a high level specification However widespread use of formal methods has had to await breakthroughs in automated reasoning integration with engineering design languages and processes scalability and usability This book presents several breakthrough design and verification techniques that allow these powerful formal methods to be employed in the real world of high assurance microprocessor system design *Formal Verification of VLIW Microprocessors with Speculative Execution* Miroslav N. Velev,2000 Abstract This is a study of the formal verification of a VLIW microprocessor that imitates the Intel Itanium 9 12 17 in features such as predicated execution register remapping advanced and speculative loads and branch prediction The formal verification is done with the Burch and Dill flushing technique 5 by exploiting the properties of Positive Equality 3 4 The contributions include an extensive use of conservative approximations in abstracting portions of the processor and a framework for decomposition of the Boolean evaluation of the correctness formula The conservative approximations are applied automatically when abstracting a memory whose forwarding logic is not affected by stalling conditions that preserve the correctness of the memory semantics for the same memory These techniques allow a reduction of more than a factor of 4 in the CPU time for the formal verification of the most complex processor model examined relative to the monolithic evaluation of the correctness formula for a version of the same processor where conservative approximations are not applied *Advanced Automation in Formal Verification of Processors* Ulrich Kühne,2009 **Formal Verification of Pipelined Microprocessors** Daniel Kroening,2004 **Progressive Automated Formal Verification of Memory Consistency in Parallel Processors** Yatin Avdhut Manerkar,2021 In recent years single threaded hardware performance has stagnated due to transistor level limitations stemming from the end of Moore s Law and Dennard scaling Instead today s designs improve performance through heterogeneous parallelism the use of multiple distinct processing elements on a chip many of which are specialised to run specific workloads The processing elements in such architectures often communicate and synchronise with each other via loads and stores to shared memory

Memory consistency models MCMs specify the ordering rules for such loads and stores MCM verification is thus critical to parallel system correctness but is notoriously hard to conduct and requires examining a vast number of scenarios Verification using formal methods can provide strong correctness guarantees based on mathematical proofs and is an excellent fit for MCM verification This dissertation makes several contributions to automated formal hardware MCM verification bringing such techniques much closer to being able to handle real world architectures Firstly my RTLCheck work enables the automatic linkage of formal models of design orderings to RTL processor implementations This linkage helps push the correctness guarantees of design time formal verification down to taped out chips The linkage doubles as a method for verifying microarchitectural model soundness against RTL Secondly my RealityCheck work enables scalable automated formal MCM verification of hardware designs by leveraging their structural modularity It also facilitates the modular specification of design orderings by the various teams designing a processor Thirdly my PipeProof work enables automated all program hardware MCM verification A processor must respect its MCM for all possible programs and PipeProof enables designers to prove such results automatically This dissertation also proposes Progressive Automated Formal Verification a novel generic verification flow Progressive verification emphasises the use of automated formal verification at multiple points in system development starting at early stage design and the linkage of the various verification methods to each other Progressive verification has multiple benefits including the earlier detection of bugs reduced verification overhead and reduced development time The combination of PipeProof RealityCheck and RTLCheck enables the progressive verification of MCM properties in parallel processors and serves as a reference point for the development of future progressive verification flows   Formal Verification of a Commercial Microprocessor SRI International. Computer Science Laboratory,Mandayam K. Srivas,Steven P. Miller,1995 Abstract Formal specification combined with mechanical verification is a promising approach for achieving the extremely high levels of assurance required of safety critical digital systems However many questions remain regarding their use in practice Can these techniques scale up to industrial systems where are they likely to be useful and how should industry go about incorporating them into practice This report discusses a project undertaken to answer some of these questions the formal verification of the AAMP5 microprocessor This project consisted of formally specifying in the PVS language a Rockwell proprietary microprocessor at both the instruction set and register transfer levels and using the PVS theorem prover to show that the microcode correctly implemented the instruction level specification for a representative subset of instructions Notable aspects of this project include the use of a formal specification language by practicing hardware and software engineers the integration of traditional inspections with formal specifications and the use of a mechanical theorem prover to verify a portion of a commercial pipelined microprocessor that was not explicitly designed for formal verification

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